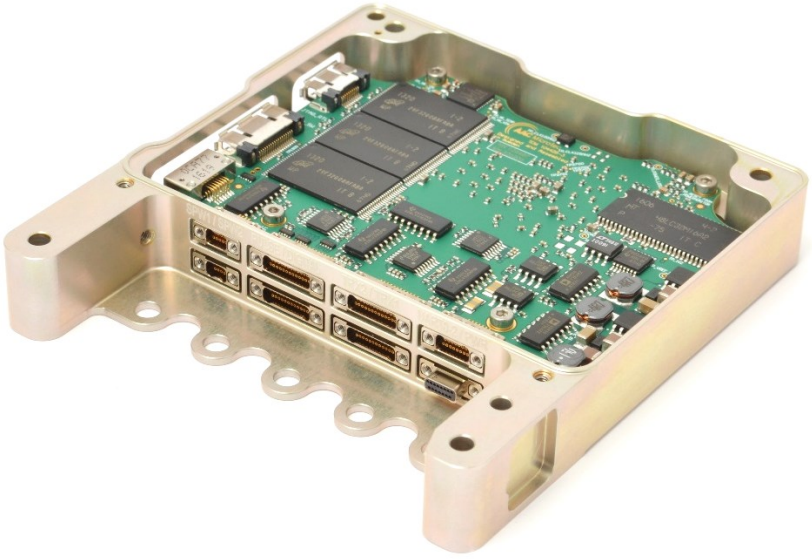
ICD – Sirius TCM

F



REVISION LOG

Rev	Date	Change description
A	2017-01-12	Released version
B	2017-10-03	Released version
C	2017-11-28	Released version
D	2018-06-21	Released version D with the following updates: - Figure 2, mechanical hole dimension added - Added TC and TM timing diagrams - Clarifications on I/O specifications
E	2019-06-05	Update of SpaceWire connector pinout
F	2020-11-26	Add information on screws and torques.

TABLE OF CONTENT

1 Introduction

This ICD is written for electrical and mechanical engineers using the ÅAC Sirius products. For software interface descriptions please see the Sirius Product User Manual document [RD1].

1.1 Reference documents

RD#	Document ref	Document name
RD1	205065	Sirius Product User Manual
RD2	104438	TCM-S Product step file

1.2 Acronyms and abbreviations

Acronym	Description
ADC	Analog to Digital Converter
CoM	Center of Mass
ESD	Electro Static Discharge
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit communication
ICD	Interface Control Document
MoI	Moment of Inertia
LVDS	Low-voltage differential signaling
OBC	OnBoard Computer
PPS	Pulse Per Second
PSU	Power Supply Unit
SPI	Serial Peripheral Interface
SpW	SpaceWire
TBD	To Be Defined
TCM	TT&C Control Module
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter

2 Mechanical ICD

2.1 General

All products in the Sirius product family share the same aluminum case. The case is designed to be configured as a stack that fits within the form factor of the CubeSat (PC104) standard. The Sirius OBC step file [RD2] provides a detailed representation of the mechanical form factor.

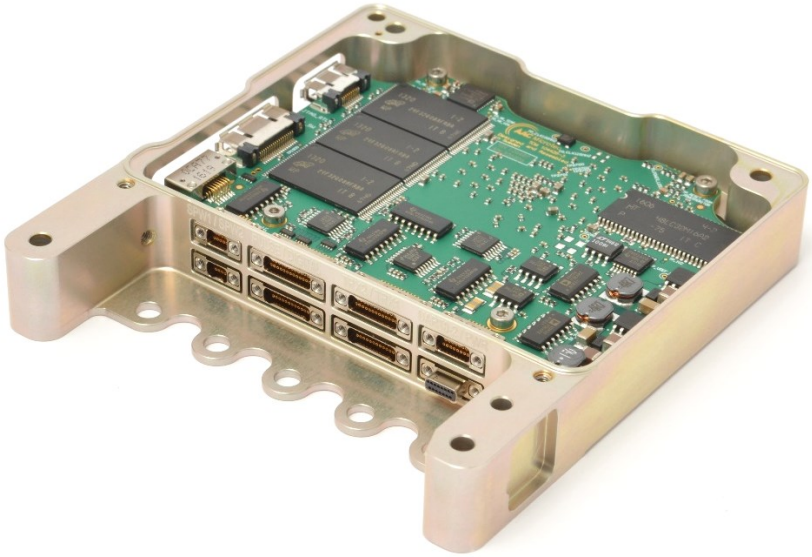


Figure 1 The Sirius TCM product without a lid

2.2 Physical properties

Property	Value	Units
Mass	132.6	gram
Volume	49286	mm²
Surface area	72910	mm²

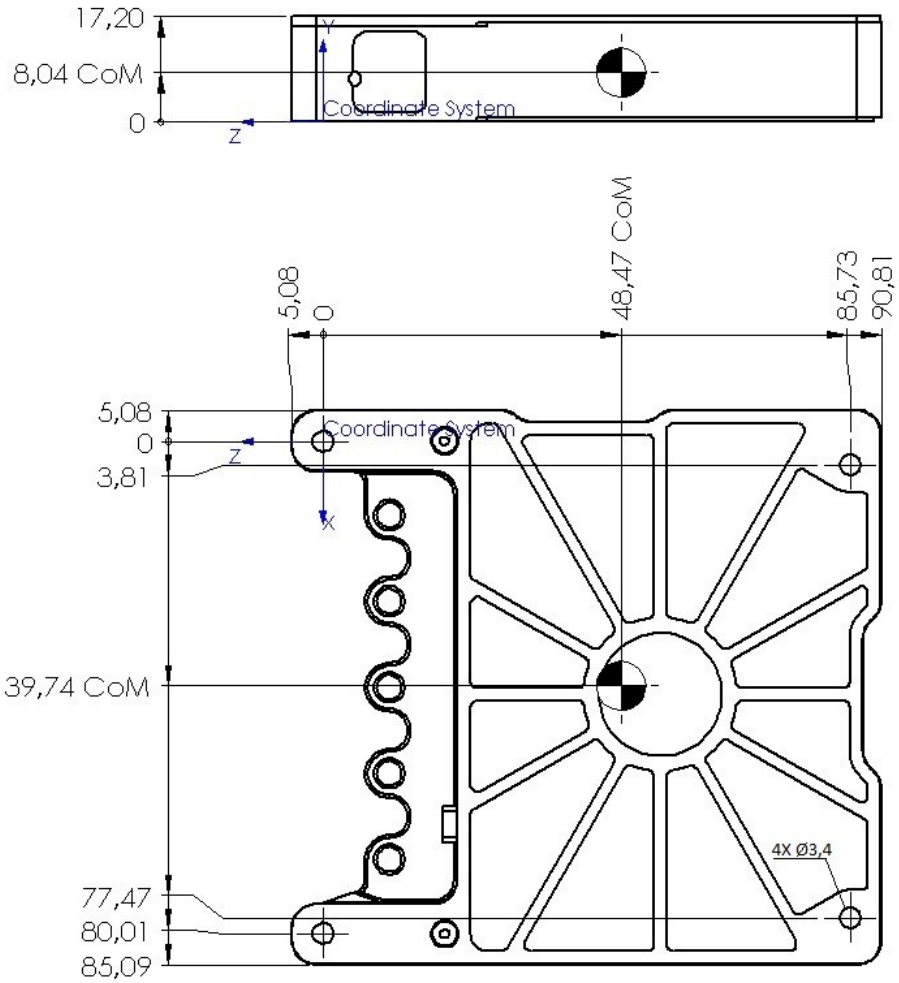


Figure 2 The dimensions of the Sirius TCM product, all measurements in mm

2.3 Center of Mass

The center of mass (CoM) is identified in Figure 2 with the origin and direction of the coordinate system indicated by the blue text.

AXIS	Center Of Mass [mm]
X	39.74
Y	8.04
Z	-48.47

2.4 Moment of inertia

The moment of inertia (MoI) for the mechanical structure is defined by the table below using the coordinate system origin is defined by Figure 2.

MOMENTS OF INERTIA [g*mm²]					
Principal axes of inertia and principal moments of inertia taken at the center of mass.		Taken at the center of mass and aligned with the output coordinate system.		Taken at the output coordinate system.	
Ix	(0.98, 0.00, 0.22)	**Lxx**	98042	**Ixx**	418127
Iy	(0.22, 0.00, -0.98)	**Lyx**	-105	**Iyx**	42254
Iz	(0.00, 1.00, 0.00)	**Lzx**	4610	**Izx**	-250813
Px	97026	**Lxy**	-105	**Ixy**	42254
Py	118973	**Lyy**	208699	**Iyy**	729647
Pz	208700	**Lzy**	-278	**Izy**	-51941
		Lxz	4610	**Ixz**	-250813
		Lyz	-278	**Iyz**	-51941
		Lzz	117959	**Izz**	335958

2.5 Mechanical resonance frequencies

Mode	Frequency [Hz]
1	563.55
2	681.58
3	876.37
4	1231.9
5	1355.8

2.6 Thermal dissipation

The primary thermal interface area of the unit is the flat surface on the +x face of the unit as shown in Figure 2 and marked blue in Figure 3. The maximum allowed temperature at the thermal interface is 60°C, this figure is what has been used for design analysis and exceeding it will violate component derating rules. The size of the thermal interface area is 1212.75 mm^2.

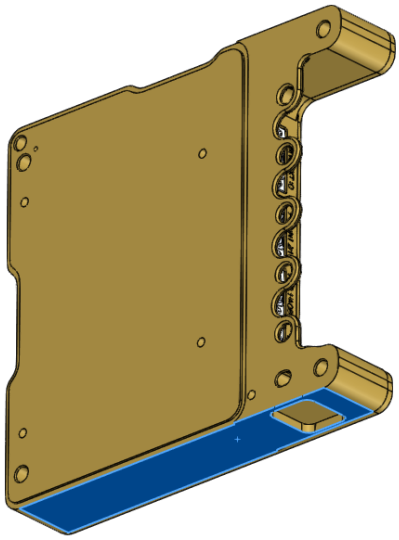


Figure 3 The Sirius products thermal interface

To aid in thermal transfer between the Sirius TCM and the surface to which it is mounted, a thermal interface pad is recommended to be placed between Sirius TCM and the spacecraft structure. The recommended TIM is Parker Cho-Therm 1671.

2.7 Screws and torques

The lid and debug hatch on the Sirius TCM are held in place with countersunk M2x6 A4-70 screws, two for the lid and three for the debug hatch. All screws shall be torqued to 0.25 Nm.

2.8 Coating

The unit is surface treated with Alodine 1200S providing corrosion resistance and electrical surface conductivity. Surfaces have an emissivity (ε) of 0.068 and absorptivity (α) of 0.15.

3 Electrical ICD

Figure 4 illustrates the locations of all Sirius TCM connectors.

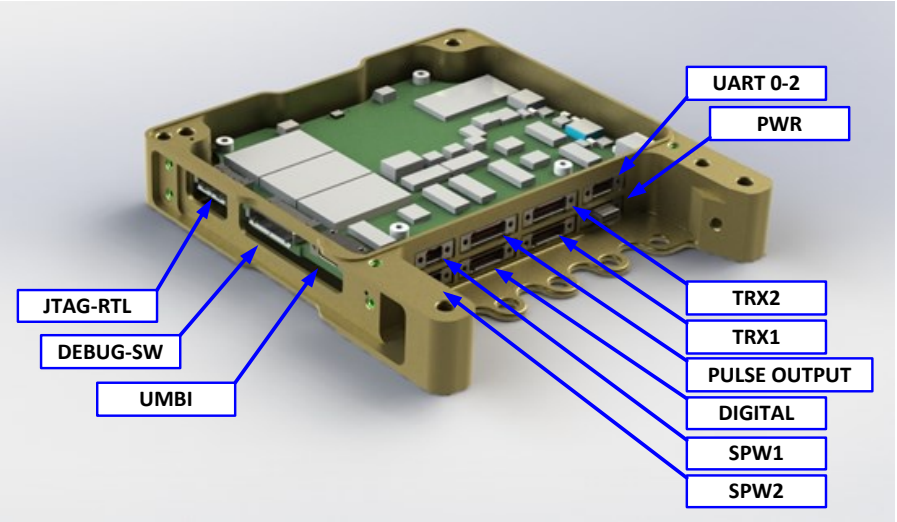


Figure 4 The connectors of the Sirius TCM product

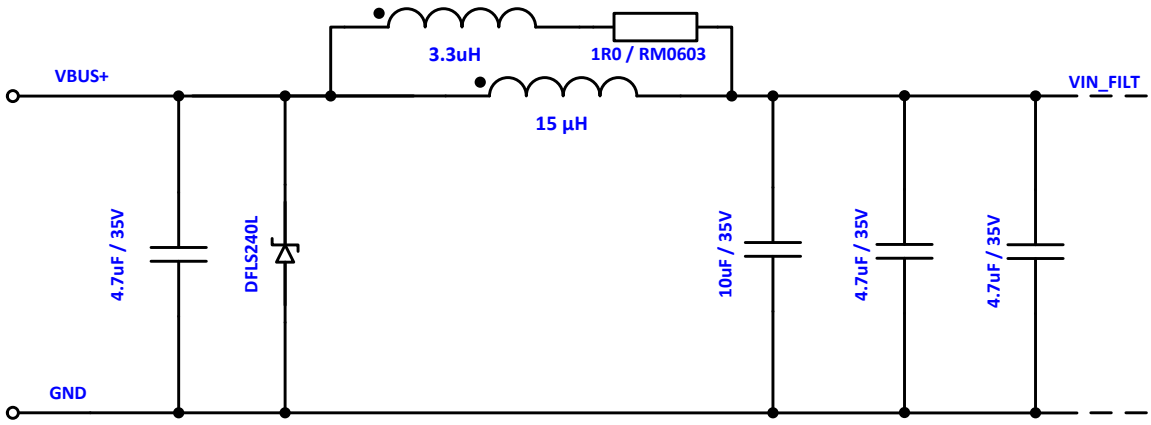
Note: All differential interfaces define the P/N signals as a one (1) if P is positive and N is negative.

3.1 PWR connector

This connector provides the input power for the unit, as well as PPS interfaces, pulse commands and safe mode communication interfaces.

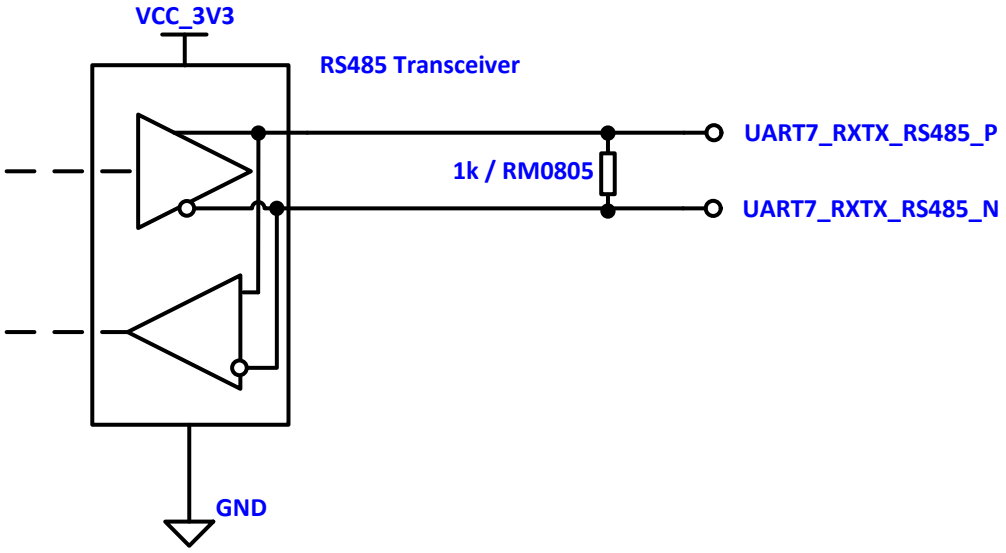
nanoD15 Plug Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	VBUS+	Power input
Pin 2	VBUS+	
Pin 3	UART7_RXTX_RS485_P	UART7 (SAFEBUS, RS485)
Pin 4	UART7_RXTX_RS485_N	
Pin 5	PPS_RS422_P	PPS transceiver
Pin 6	PPS_RS422_N	
Pin 7	UART6_RXTX_RS485_P	UART6 (PSU control, RS485)
Pin 8	UART6_RXTX_RS485_N	
Pin 9	GND	Ground
Pin 10	GND	
Pin 11	GND	
Pin 12	PULSE0_I_RS422_P	Pulse Command 0
Pin 13	PULSE0_I_RS422_N	
Pin 14	PULSE1_I_RS422_P	Pulse Command 1
Pin 15	PULSE1_I_RS422_N	

3.1.1 VBUS - Power input



NAME	DESCRIPTION	PINS	VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [A]	MAX [A]
VBUS+	Power input	1, 2	+4.5	+16.0	0	0.6
GND	Power return	9, 10, 11	0	0.1	0	0.6

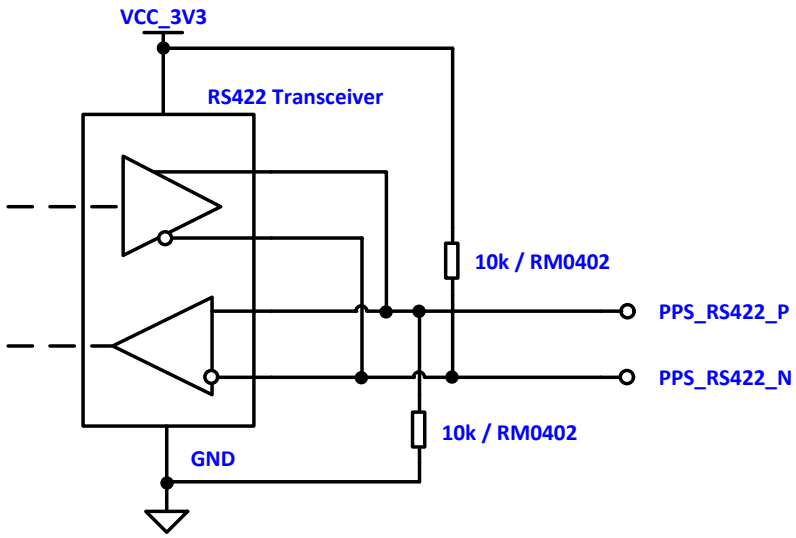
3.1.2 UART7 - SAFEBUS



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART7_RXTX_RS485_P	SAFEBUS Output mode	3	2.0	0	0.4	2.4	3.6	-20	+20
UART7_RXTX_RS485_N		4		0	0.4	2.4	3.6	-20	+20
UART7_RXTX_RS485_P	SAFEBUS Input mode	3	0.2	-7	-	-	+12	-3.6	+3.6
UART7_RXTX_RS485_N		4		-7	-	-	+12	-3.6	+3.6

3.1.3 PPS transceiver

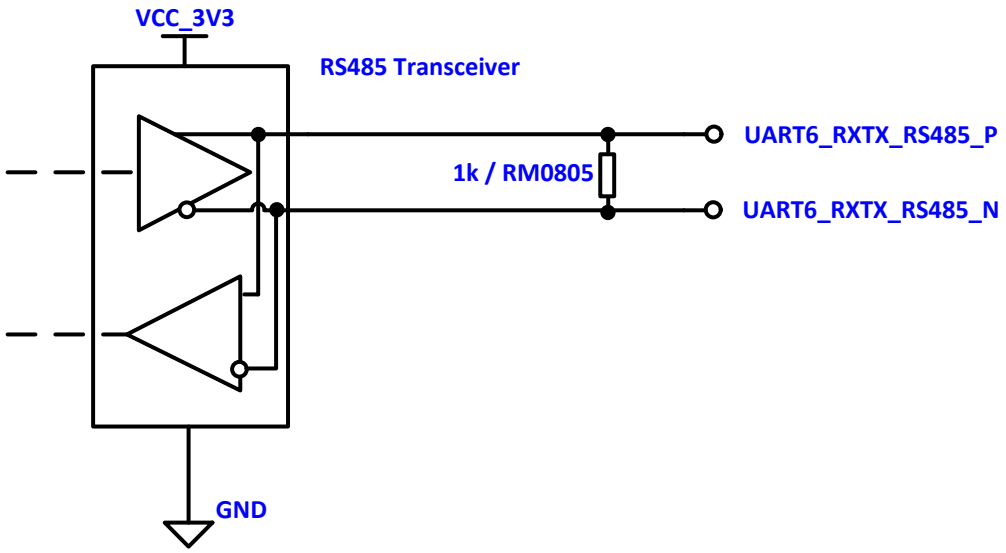
To provide external time synchronization, a PPS input-only is provided as defined in section 3.8.1. The PPS transceiver input can act as both a distributor and receiver of the PPS, user configurable.



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
PPS_RS422_P	PPS Output mode	5	2.0	0	+0.4	+2.4	+3.6	-20	+20
PPS_RS422_N		6		0	+0.4	+2.4	+3.6	-20	+20
PPS_RS422_P	PPS Input mode	5	0.2	-7	-	-	+12	-3.6	+3.6
PPS_RS422_N		6		-7	-	-	+12	-3.6	+3.6

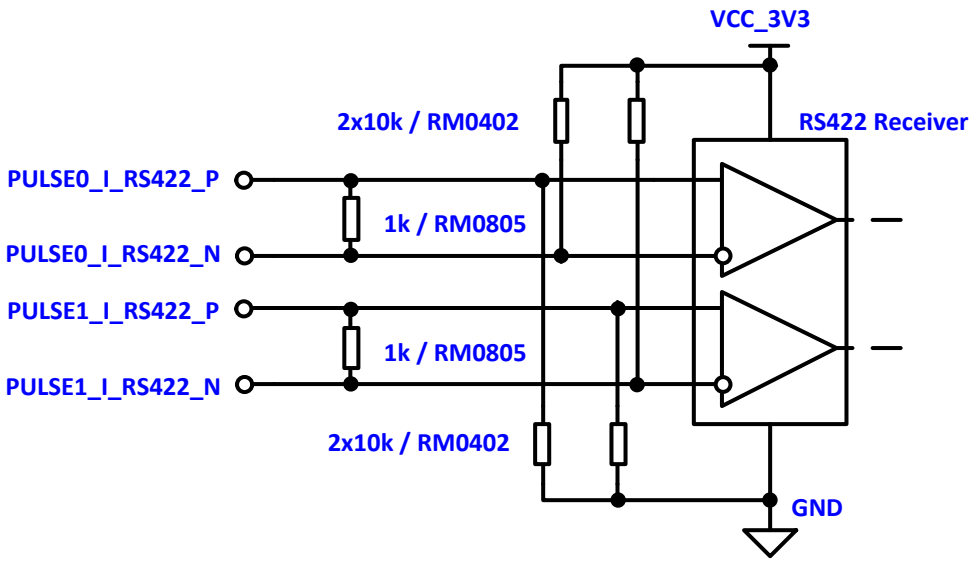
Note: the PPS pulse shall be within 1 us – 1 ms time window with differential RS422 voltage levels. A valid PPS pulse shall be logic high.

3.1.4 UART6 - PSU Control



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART6_RXTX_RS485_P	PSU CTRL Output mode	7	2.0	0	0.4	2.4	3.6	-20	+20
UART6_RXTX_RS485_N		8		0	0.4	2.4	3.6	-20	+20
UART6_RXTX_RS485_P	PSU CTRL Input mode	7	0.2	-7	-	-	+12	-3.6	+3.6
UART6_RXTX_RS485_N		8		-7	-	-	+12	-3.6	+3.6

3.1.5 PULSE command input



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]
PULSE0_I_RS422_P	Pulse Command Input	12	0.2	-7	-	-	+7
PULSE0_I_RS422_N		13		-7	-	-	+7
PULSE1_I_RS422_P	Pulse Command Input	14	0.2	-7	-	-	+7
PULSE1_I_RS422_N		15		-7	-	-	+7

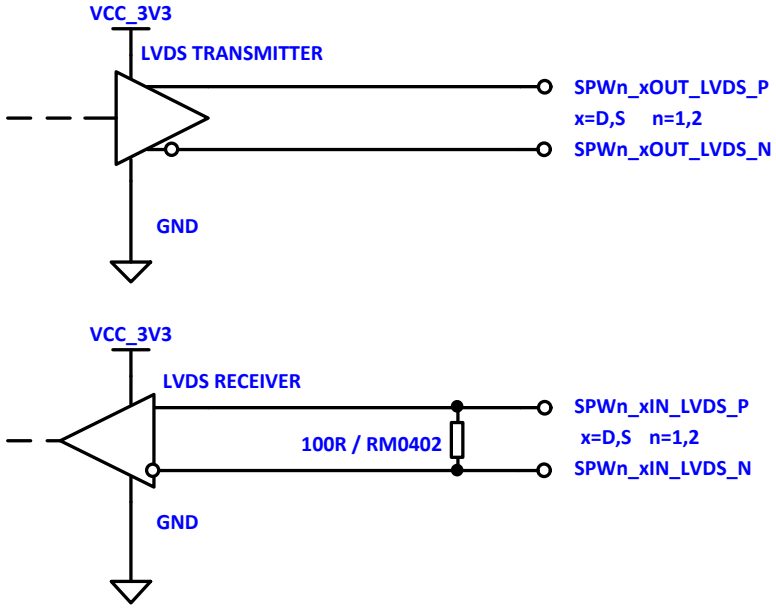
Note: A valid pulse command shall have a minimum length of 20 ms and a maximum length of 40 ms. The pulse shall have differential RS422 levels. A valid pulse command shall have both a rising edge and a falling edge, in that order.

3.2 SPW1 connector

This connector contains one of the two SpaceWire communications interfaces.

nanoD9 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	SPW1_DIN_LVDS_P	Data in, Positive
Pin 2	SPW1_SIN_LVDS_P	Strobe in, Positive
Pin 3	CGND[1]	Chassis ground[1]
Pin 4	SPW1_SOUT_LVDS_N	Strobe out, Negative
Pin 5	SPW1_DOUT_LVDS_N	Data out, Negative
Pin 6	SPW1_DIN_LVDS_N	Data in, Negative
Pin 7	SPW1_SIN_LVDS_N	Strobe in, Negative
Pin 8	SPW1_SOUT_LVDS_P	Strobe out, Positive
Pin 9	SPW1_DOUT_LVDS_P	Data out, Positive

Note 1: Pin 3 can be connected to CGND or NC, depending on hardware configuration. Both have equivalent EMI and signal integrity performance.



NAME	DESCRIPTION	CONNECTOR PINS	DIFF. VOLTAGE		LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
SPW1_DIN_LVDS_P	Data in	1	0.1	1.8	0	-	-	3.3	-17	17
SPW1_DIN_LVDS_N		6			0	-	-	3.3	-17	17
SPW1_SIN_LVDS_P	Strobe in	2	0.1	1.8	0	-	-	3.3	-17	17
SPW1_SIN_LVDS_N		7			0	-	-	3.3	-17	17
SPW1_DOUT_LVDS_P	Data out	9	0.25		0.9	-	-	1.6	-6.0	6.0
SPW1_DOUT_LVDS_N		5			0.9	-	-	1.6	-6.0	6.0
SPW1_SOUT_LVDS_P	Strobe out	8	0.25		0.9	-	-	1.6	-6.0	6.0

SPW1_SOUT_LVDS_N		4			0.9	-	-	1.6	-6.0	6.0

3.3 SPW2 connector

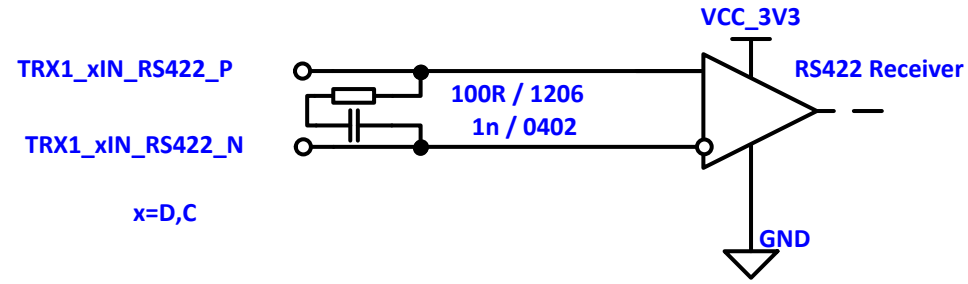
The SPW2 – SpaceWire signal names and signal behavior are the same as described in section 3.2. Signal index names are changed from SPW1 to SPW2. The electrical interface schematics are identical to those shown in section 3.2.

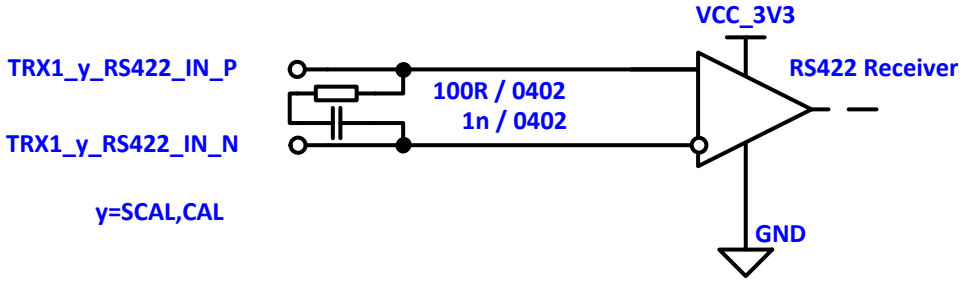
3.4 TRX1 connector

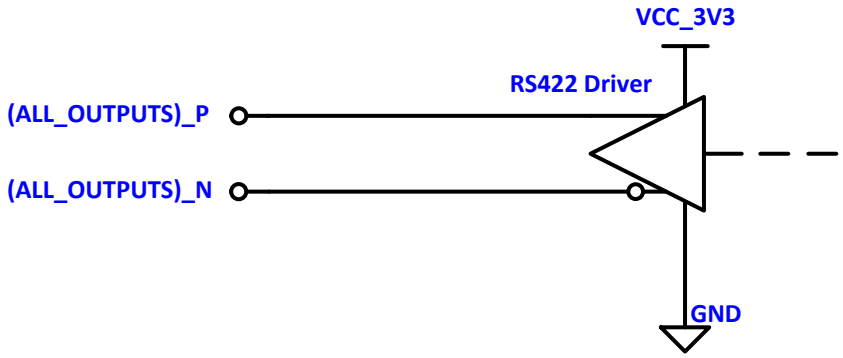
This connector provides the RS422-level radio interface. The RS422 interface supports up to 400 kBaud signaling rate before violating the power derating for the termination resistor.

nanoD25 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	TRX1_DOUT_RS422_P	RS422 level baseband data out
Pin 2	TRX1_DOUT_RS422_N	
Pin 3	TRX1_COUT_RS422_P	RS422 level baseband clock out
Pin 4	TRX1_COUT_RS422_N	
Pin 5	TRX1_DIN_RS422_P	RS422 level baseband data in
Pin 6	TRX1_DIN_RS422_N	
Pin 7	TRX1_CIN_RS422_P	RS422 level baseband clock in
Pin 8	TRX1_CIN_RS422_N	
Pin 9	TRX1_SCAL_IN_ RS422_P	RS422 level sub-carrier lock in Defined as active low
Pin 10	TRX1_SCAL_IN_ RS422_N	
Pin 11	TRX1_CAL_IN_ RS422_P	RS422 level carrier lock in. Defined as active low
Pin 12	TRX1_CAL_IN_ RS422_N	
Pin 13	GND	Ground
Pin 14	GND	
Pin 15	GND	
Pin 16	GND	
Pin 17	GND	
Pin 18	GND	
Pin 19	GND	
Pin 20	UART4_TX_RS422_P	RS422 Output
Pin 21	UART4_TX_RS422_N	
Pin 22	UART4_RX_RS422_P	RS422 Input
Pin 23	UART4_RX_RS422_N	
Pin 24	GND	Ground
Pin 25	GND	Ground

3.4.1 TRX1 – RS422



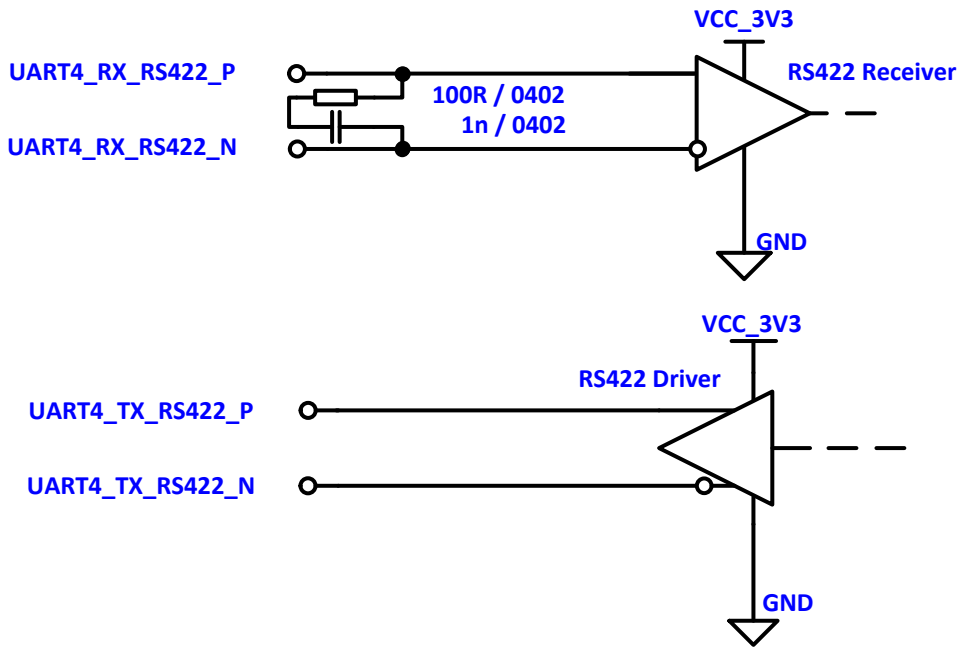




NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
TRX1_(DIN, CIN)_RS422_P	RS422 Input	5,7	0.2	-7	-	-	7	-60	+60
TRX1_(DIN, CIN)_RS422_N		6,8		-7	-	-	7	-60	+60
TRX1_(SCAL_IN, CAL_IN)_RS422_P		9,11	0.2	-7	-	-	7	-60	+60
TRX1_(SCAL_IN, CAL_IN)_RS422_N		10,12		-7	-	-	7	-60	+60
(ALL_OUTPUTS)_P	RS422 Output	1,3	2.0	0	-	-	3.6	-30	+30
(ALL_OUTPUTS)_N		2,4		0	-	-	3.6	-30	+30

Note: This denotes the peak AC current into the AC termination. Steady state DC current is max. ±150 µA.

3.4.2 UART4 – RS422



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART4_RX_RS4XX_P	UART4 RX	22	0.2	-7	-	-	7	-60	+60
UART4_RX_RS4XX_N		23		-7	-	-	7	-60	+60
UART4_TX_RS4XX_P	UART4 TX	20	2.0	0	0.4	2.4	3.6	-30	+30
UART4_TX_RS4XX_N		21		0	0.4	2.4	3.6	-30	+30

Note: This denotes the peak AC current into the AC termination. Steady state DC current is max. +/-700µA.

3.4.3 TM interface

Figure 5 details the output timing between the clock (COUT) and data (DOUT) on the TM interface. Depending on the radio used and how that samples data, the harness needs to be adjusted to match. I.e. for a radio that samples data on the **falling edge** of the clock input (COUT) the default harness configuration can be used (TCM_COUT_P <-> RADIO_CIN_P, TCM_COUT_N <-> RADIO_CIN_N). However, if the radio samples the data on the **rising edge**, the TM_COUT P and N signals needs to be switched in the connection between the radio and the TCM (TCM_COUT_N <-> RADIO_CIN_P, TCM_COUT_P <-> RADIO_CIN_N).

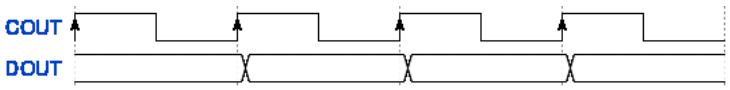


Figure 5 TM default clock and data timing diagram

3.4.4 TC interface

Figure 6 details the expected input timing between the clock (CIN) and data (DIN) together with the subcarrier lock signal (SCAL_IN) on the TC interface. Just as for the TM interface, different radios might change the data on different clock flanks. As the TCM TC interface

samples data on the **rising edge** of the clock (CIN), P and N signals might need switching here as well. The setup and hold times should be at least 1/4th clock cycle each. When the subcarrier lock signal (SCAL_IN) is high, any data on the TC interface will be ignored.

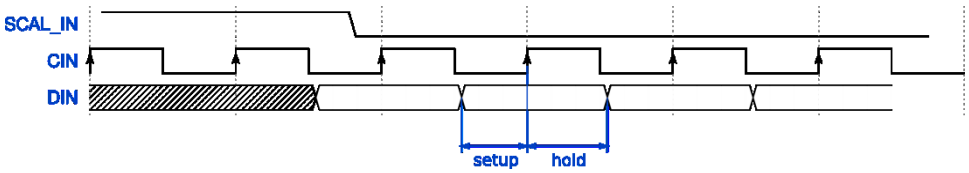


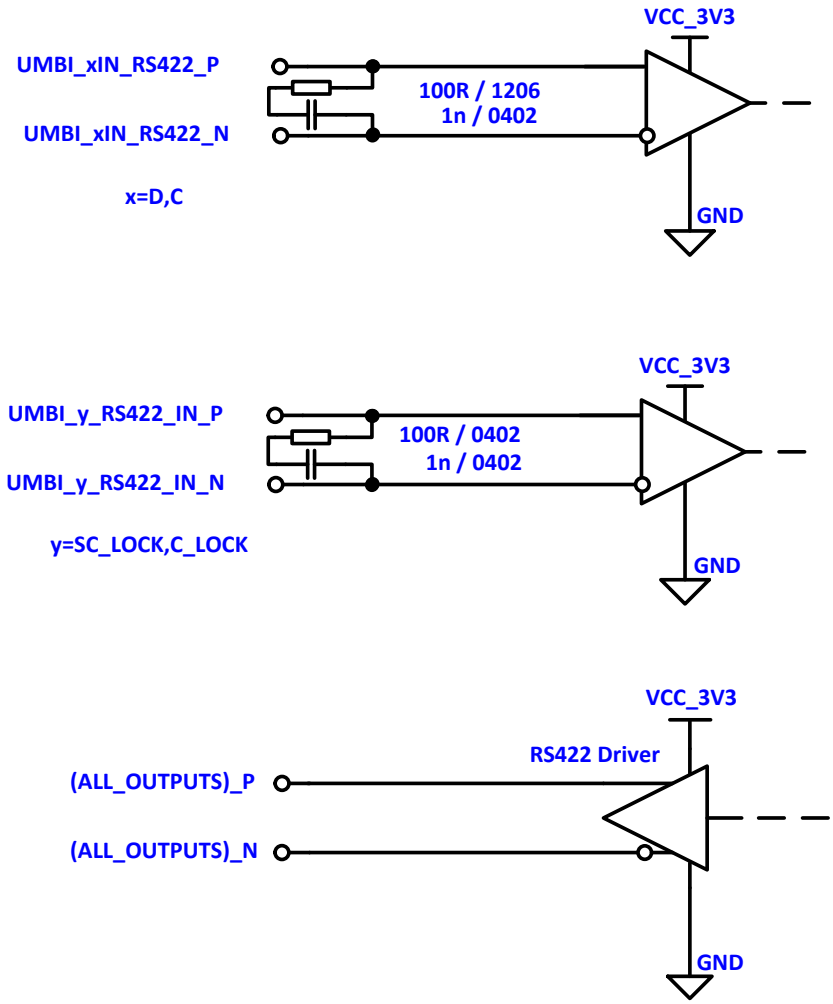
Figure 6 TC default clock, data and subcarrier lock timing diagram

3.5 UMBI connector

This connector is used for sending simulated radio (CCSDS) data through an umbilical connection. Please see sections 3.4.3 and 3.4.4 for clock and data signaling polarization. The RS422 UMBI interface supports up to 400 kBaud signaling rate before violating the power derating for the termination resistor.

nanoD15 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	UMBI_DOUT_RS422_P	RS422 level baseband data out
Pin 2	UMBI_DOUT_RS422_N	
Pin 3	UMBI_COUT_RS422_P	RS422 level baseband clock out
Pin 4	UMBI_COUT_RS422_N	
Pin 5	UMBI_DIN_RS422_P	RS422 level baseband data in
Pin 6	UMBI_DIN_RS422_N	
Pin 7	UMBI_CIN_RS422_P	RS422 level baseband clock in
Pin 8	UMBI_CIN_RS422_N	
Pin 9	UMBI_SC_LOCK_IN_ RS422_P	RS422 level sub-carrier lock in. Defined as active low
Pin 10	UMBI_SC_LOCK_IN_ RS422_N	
Pin 11	UMBI_C_LOCK_IN_ RS422_P	RS422 level carrier lock in Defined as active low
Pin 12	UMBI_C_LOCK_IN_ RS422_N	
Pin 13	UMBI_DETECT	Detects the umbilical connection with an active low signal
Pin 14	GND	Ground
Pin 15	GND	Ground

3.5.1 Umbilical data interface



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UMBI_(DIN, CIN)_RS422_P	RS422 Input	5,7	0.2	-7	-	-	7	-60	+60
UMBI_(DIN, CIN)_RS422_N		6,8		-7	-	-	7	-60	+60
UMBI_(SC_LOCK_IN, C_LOCK_IN)_RS422_P		9,11	0.2	-7	-	-	7	-60	+60
UMBI_(SC_LOCK_IN, C_LOCK_IN)_RS422_N		10,12		-7	-	-	7	-60	+60
(ALL_OUTPUTS)_P	RS422 Output	1,3	2.0	0	-	-	3.6	-30	+30
(ALL_OUTPUTS)_N		2,4		0	-	-	3.6	-30	+30

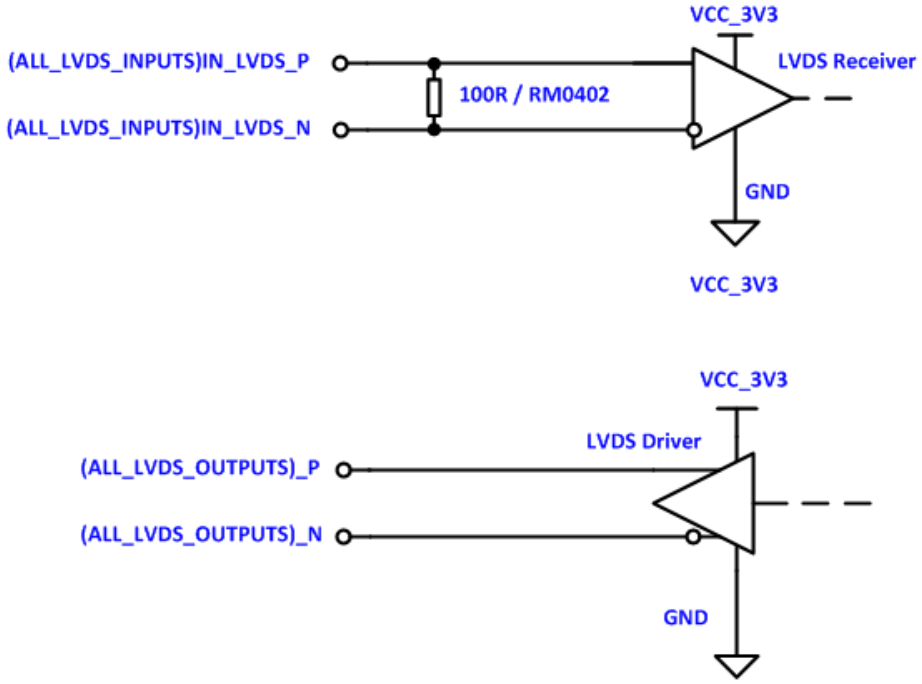
Note: This denotes the peak current into the AC termination. Steady state DC current is max ±150µA.

3.6 TRX2 connector

This connector provides the LVDS-level radio interface. Please see sections 3.4.3 and 3.4.4 for clock and data signaling polarization.

nanoD25 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	TRX2_DOUT_LVDS_P	Baseband data out, LVDS
Pin 2	TRX2_DOUT_LVDS_N	
Pin 3	TRX2_COUT_LVDS_P	Baseband clock out, LVDS
Pin 4	TRX2_COUT_LVDS_N	
Pin 5	TRX2_DIN_LVDS_P	Baseband data in, LVDS
Pin 6	TRX2_DIN_LVDS_N	
Pin 7	TRX2_CIN_LVDS_P	Baseband clock in, LVDS
Pin 8	TRX2_CIN_LVDS_N	
Pin 9	TRX2_SCAL_IN_LVDS_P	Sub-carrier lock in, LVDS Defined as active low
Pin 10	TRX2_SCAL_IN_LVDS_N	
Pin 11	TRX2_CAL_IN_LVDS_P	Carrier lock in, LVDS. Defined as active low
Pin 12	TRX2_CAL_IN_LVDS_N	
Pin 13	GND	Ground
Pin 14	UART3_TX_LVDS_P	TRX control & housekeeping signaling, LVDS
Pin 15	UART3_TX_LVDS_N	
Pin 16	UART3_RX_LVDS_P	TRX control & housekeeping signaling, LVDS
Pin 17	UART3_RX_LVDS_N	
Pin 18	GND	Ground
Pin 19	GND	
Pin 20	UART3_TX_RS422_P	TRX control & housekeeping signaling, RS422
Pin 21	UART3_TX_RS422_N	
Pin 22	UART3_RX_RS422_P	TRX control & housekeeping signaling, RS422
Pin 23	UART3_RX_RS422_N	
Pin 24	TRX2_DETECT	NOT USED in FM
Pin 25	GND	Ground

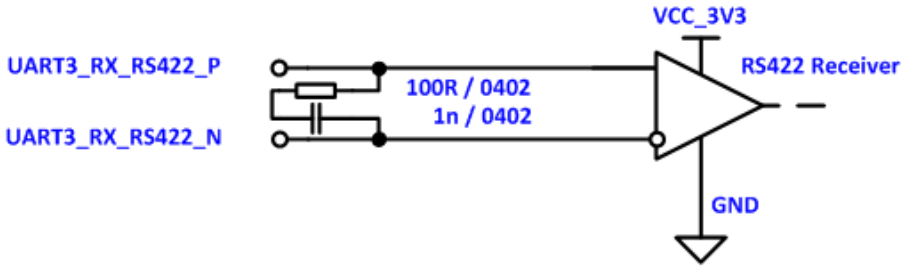
3.6.1 TRX2 – LVDS

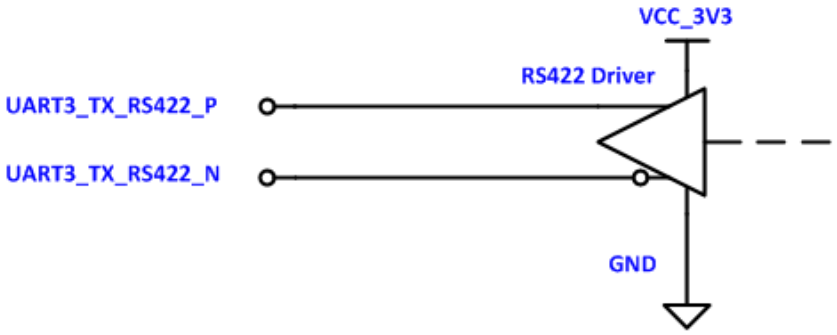


NAME	DESCRIPTION	PINS	DIFF. VOLTAGE		LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
(ALL_LVDS_INPUTS)IN_LVDS_P	LVDS Input	5,7,9,11	0.1	1.8	0	-	-	3.3	-17	17
(ALL_LVDS_INTPUTS)IN_LVDS_N		6,8,10,12			0	-	-	3.3	-17	17
(ALL_LVDS_OUTPUTS)_P	LVDS Output	1,3	0.25		0.9	-	-	1.6	-6.0	6.0
(ALL_LVDS_OUTPUTS)_N		2,4			0.9	-	-	1.6	-6.0	6.0

3.6.2 UART3 – RS422

This interface is applicable to control and read the housekeeping RS422 data provided by the TRX2 radio equipment. The RS422 input supports up to 400 kBaud signaling rate before violating the power derating for the termination resistor.



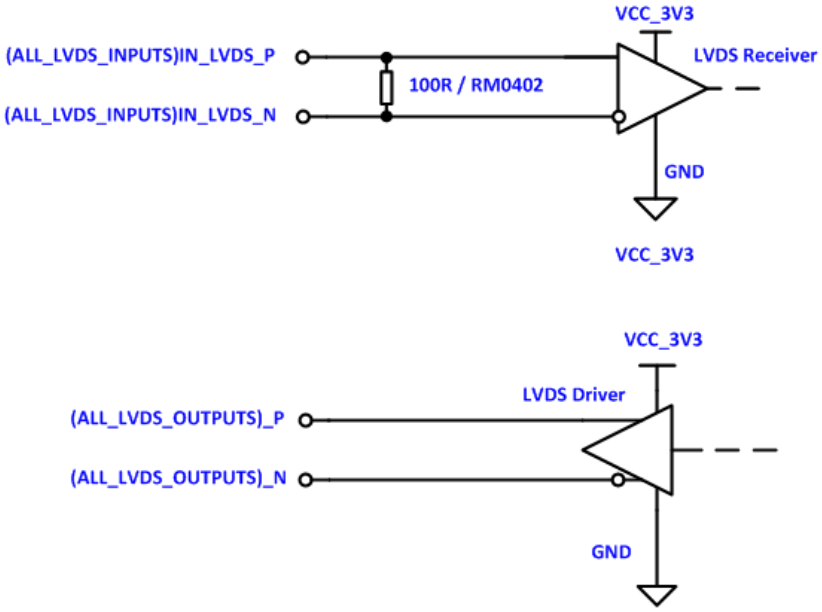


NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART3_RX_RS4XX_P	UART3 RX RS4XX	22	0.2	-7	-	-	7	-60	+60
UART3_RX_RS4XX_N		23		-7	-	-	7	-60	+60
UART3_TX_RS4XX_P	UART3 TX RS4XX	20	2.0	0	0.4	2.4	3.6	-30	+30
UART3_TX_RS4XX_N		21		0	0.4	2.4	3.6	-30	+30

Note: This denotes the peak current into the AC termination. Steady state DC current is max ±150µA.

3.6.3 UART3 – LVDS

This interface is applicable to control and read the housekeeping LVDS data provided by the TRX2 radio equipment.

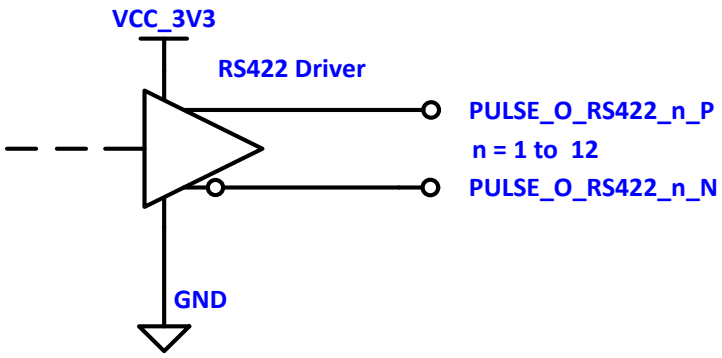


NAME	DESCRIPTION	PINS	DIFF. VOLTAGE		LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART3_RX_LVDS_P	UART3 RX LVDS	16	0.1	1.8	0	-	-	3.3	-17	17
UART3_RX _LVDS_N		17			0	-	-	3.3	-17	17
UART3_TX _LVDS_P	UART3 TX LVDS	14	0.25		0.9	-	-	1.6	-6.0	6.0
UART3_TX _LVDS_N		15			0.9	-	-	1.6	-6.0	6.0

3.7 PULSE output connector

This connector provides the PUS command controlled hardware pulse-commands. The format of the pulse command is compatible with the pulse command input present on the Sirius power connector (identical for both Sirius TCM and OBC).

nanoD25 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	PULSE_O_RS422_1_P	PULSE RS422 output #1
Pin 2	PULSE_O_RS422_1_N	
Pin 3	PULSE_O_RS422_2_P	PULSE RS422 output #2
Pin 4	PULSE_O_RS422_2_N	
Pin 5	PULSE_O_RS422_3_P	PULSE RS422 output #3
Pin 6	PULSE_O_RS422_3_N	
Pin 7	PULSE_O_RS422_4_P	PULSE RS422 output #4
Pin 8	PULSE_O_RS422_4_N	
Pin 9	PULSE_O_RS422_5_P	PULSE RS422 output #5
Pin 10	PULSE_O_RS422_5_N	
Pin 11	PULSE_O_RS422_6_P	PULSE RS422 output #6
Pin 12	PULSE_O_RS422_6_N	
Pin 13	GND	Ground
Pin 14	PULSE_O_RS422_7_P	PULSE RS422 output #7
Pin 15	PULSE_O_RS422_7_N	
Pin 16	PULSE_O_RS422_8_P	PULSE RS422 output #8
Pin 17	PULSE_O_RS422_8_N	
Pin 18	PULSE_O_RS422_9_P	PULSE RS422 output #9
Pin 19	PULSE_O_RS422_9_N	
Pin 20	PULSE_O_RS422_10_P	PULSE RS422 output #10
Pin 21	PULSE_O_RS422_10_N	
Pin 22	PULSE_O_RS422_11_P	PULSE RS422 output #11
Pin 23	PULSE_O_RS422_11_N	
Pin 24	PULSE_O_RS422_12_P	PULSE RS422 output #12
Pin 25	PULSE_O_RS422_12_N	



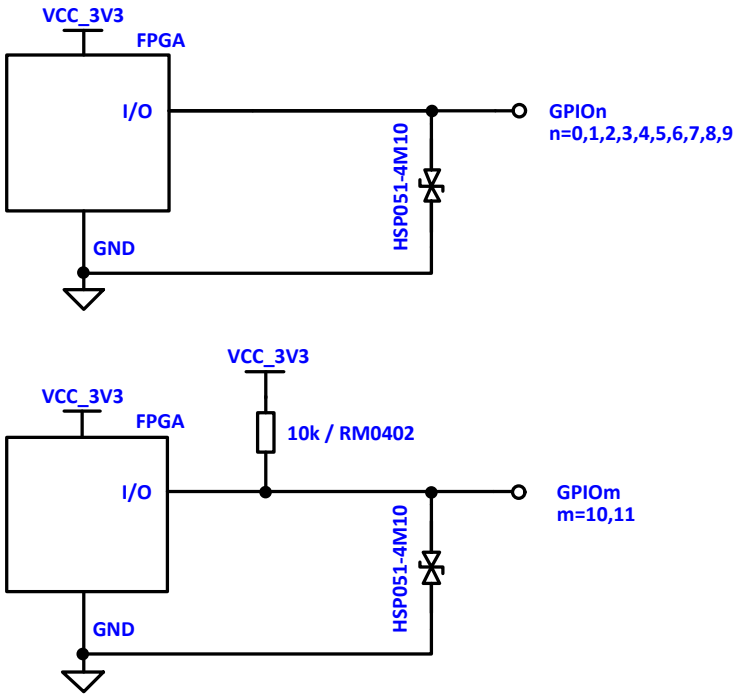
NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
PULSE_O_RS422_n_P	RS422 Output	1,3,5,7,9,11,14, 16,18,20,22,24	2.0	0	-	-	3.6	-30	+30
PULSE_O_RS422_n_N		2,4,6,8,10,12,15, 17,19,21,23,25		0	-	-	3.6	-30	+30

3.8 DIGITAL connector

This connector provides several digital I/O interfaces and an external interface for a PPS time synchronization signal.

nanoD25 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	GPIO0	LVTTL digital inputs/outputs
Pin 2	GPIO1	
Pin 3	GPIO2	
Pin 4	GPIO3	
Pin 5	GPIO4	
Pin 6	GPIO5	
Pin 7	GPIO6	
Pin 8	GPIO7	
Pin 9	GPIO8	
Pin 10	GPIO9	
Pin 11	GPIO10	LVTTL digital input/output with 10kΩ pull up resistor for open drain usage
Pin 12	GPIO11	LVTTL digital input/output with 10kΩ pull up resistor for open drain usage
Pin 13	GND	Ground
Pin 14	SPI_MISO	NOT USED
Pin 15	SPI_MOSI	
Pin 16	SPI_CLK	
Pin 17	I2C_SCL0	NOT USED
Pin 18	I2C_SDA0	
Pin 19	I2C_SCL1	NOT USED
Pin 20	I2C_SDA1	
Pin 21	I2C_SCL2	NOT USED
Pin 22	I2C_SDA2	
Pin 23	PPS_INPUT_RS422_N	PPS input, differential RS422 signal for time synchronization
Pin 24	PPS_INPUT_RS422_P	
Pin 25	GND	Ground

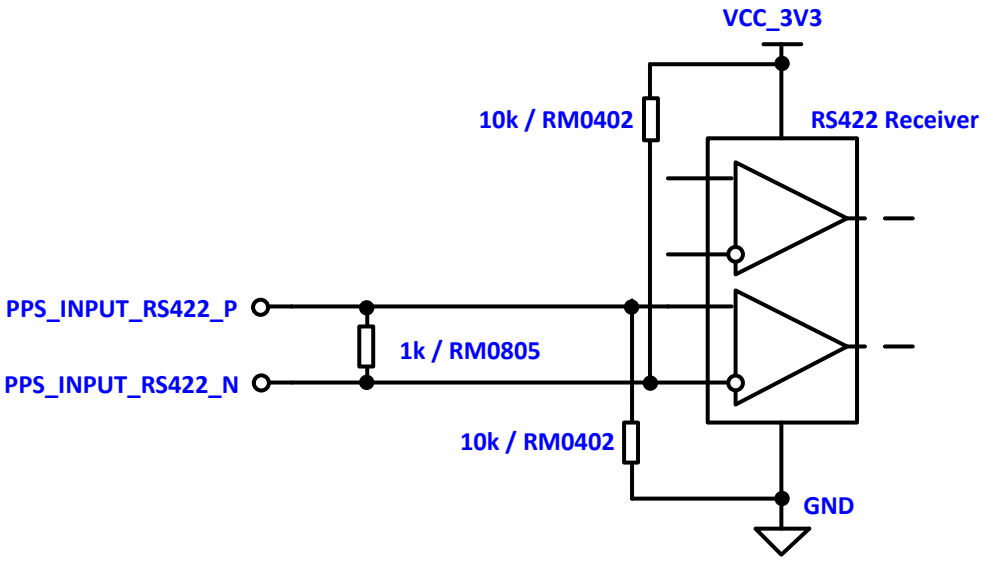
3.8.1 GPIO Interface



NAME	DESCRIPTION	CONNECTOR PINS	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
GPIOn out	GPIO configured as output	1,2,3,4,5,6,7, 8,9,10	0	0.4	2.4	3.45	-12	12
GPIOn in	GPIO configured as input	1,2,3,4,5,6,7, 8,9,10	-0.3	0.8	2.0	3.45	-0.01	0.01
GPIOn out	GPIO w/ pull-up configured as output	11,12	0	0.4	2.4	3.45	-12	12
GPIOn in	GPIO w/ pull-up configured as input	11,12	-0.3	0.8	2.0	3.45	-0.01	0.29

3.8.2 PPS Input Interface

The PPS pulse is required to be a positive pulse within 1 us – 1 ms time duration.

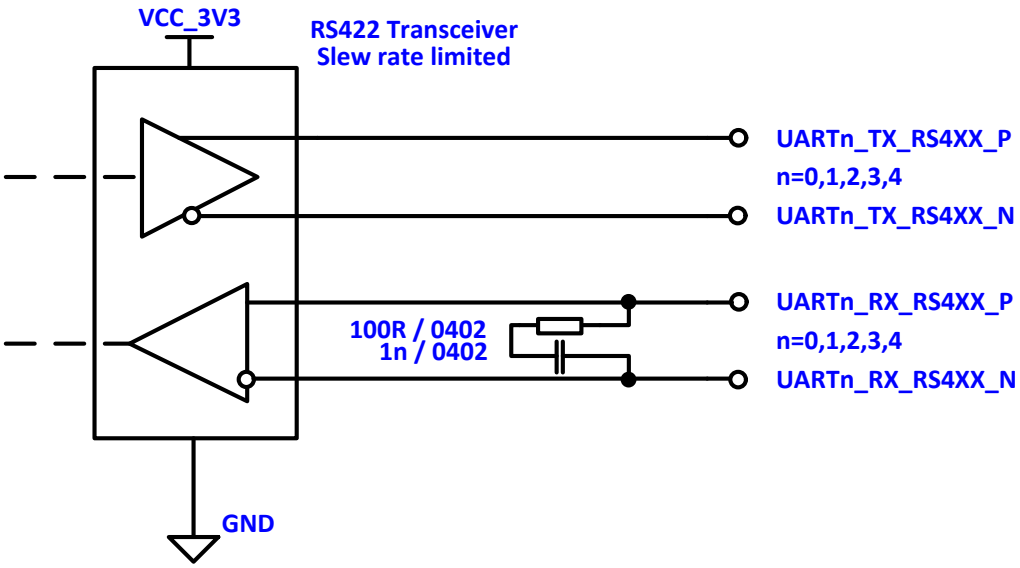


NAME	DESCRIPTION	CONNECTOR PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
PPS_INPUT_RS422_N	PPS INPUT	23	0.2	-7	-	-	7	-0.7	+1.2
PPS_INPUT_RS422_P		24		-7	-	-	7	-0.7	+1.2

3.9 UART 0-2 connector

This connector provides three RS422 UART interfaces that can also be used in RS485 configuration through connecting input and output circuits to one signal pair. The RS422/485 UARTs support up to 400 kBaud signaling rate before violating the power derating for the termination resistor.

nanoD15 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	UART0_RX_RS4XX_P	UART0 RX. For RS485 mode, connect to UART0 TX
Pin 2	UART0_RX_RS4XX_N	
Pin 3	UART0_TX_RS4XX_P	UART0 TX. For RS485 mode, connect to UART0 RX
Pin 4	UART0_TX_RS4XX_N	
Pin 5	GND	Ground
Pin 6	GND	
Pin 7	UART1_RX_RS4XX_P	UART1 RX. For RS485 mode, connect to UART1 TX
Pin 8	UART1_RX_RS4XX_N	
Pin 9	UART1_TX_RS4XX_P	UART1 TX. For RS485 mode, connect to UART1 RX
Pin 10	UART1_TX_RS4XX_N	
Pin 11	UART2_RX_RS4XX_P	UART2 RX. For RS485 mode, connect to UART2 TX
Pin 12	UART2_RX_RS4XX_N	
Pin 13	UART2_TX_RS4XX_P	UART2 TX. For RS485 mode, connect to UART2 RX
Pin 14	UART2_TX_RS4XX_N	
Pin 15	GND	Ground



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART0_RX_RS4XX_P	UART0 RX	1	0.2	-7	-	-	12	-60	+60
UART0_RX_RS4XX_N		2		-7	-	-	12	-60	+60
UART0_TX_RS4XX_P	UART0 TX	3	2.0	0	0.4	2.4	3.6	-20	+20
UART0_TX_RS4XX_N		4		0	0.4	2.4	3.6	-20	+20
UART1_RX_RS4XX_P	UART1 RX	7	0.2	-7	-	-	12	-60	+60
UART1_RX_RS4XX_N		8		-7	-	-	12	-60	+60
UART1_TX_RS4XX_P	UART1 TX	9	2.0	0	0.4	2.4	3.6	-20	+20
UART1_TX_RS4XX_N		10		0	0.4	2.4	3.6	-20	+20
UART2_RX_RS4XX_P	UART2 RX	11	0.2	-7	-	-	12	-60	+60
UART2_RX_RS4XX_N		12		-7	-	-	12	-60	+60
UART2_TX_RS4XX_P	UART2 TX	13	2.0	0	0.4	2.4	3.6	-20	+20
UART2_TX_RS4XX_N		14		0	0.4	2.4	3.6	-20	+20

Note: This denotes the peak current into the AC termination. Steady state DC current is max. +/-125µA.

3.10 JTAG-RTL connector

This connector provides an interface to program the FPGA during manufacturing.

ST60-10P connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	GND	Interface to Microsemi FlashPro programmer
Pin 2	RTL-JTAG-TDI	
Pin 3	RTL-JTAG-TRSTB	
Pin 4	VCC_3V3	
Pin 5	VCC_3V3	
Pin 6	RTL-JTAG-TMS	
Pin 7	Not connected	
Pin 8	RTL-JTAG-TDO	
Pin 9	GND	
Pin 10	RTL-JTAG-TCK	

3.11 DEBUG-SW connector

This connector provides the programming interface for the AAC debugger.

ST60-18P connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	ETH-DEBUG-RESET	Interface to AAC debugger
Pin 2	ETH-DEBUG-DETECT	
Pin 3	ETH-DEBUG-SYNC	
Pin 4	ETH-DEBUG-TX	
Pin 5	ETH-DEBUG-RX	
Pin 6	ETH-DEBUG-MDC	
Pin 7	ETH-DEBUG-MDIO	
Pin 8	ETH-DEBUG-CLK	
Pin 9	GND	
Pin 10	DEBUG-JTAG-TDI	Interface to AAC debugger
Pin 11	DEBUG-JTAG-RX	
Pin 12	DEBUG-JTAG-TX	
Pin 13	VCC_3V3	
Pin 14	DEBUG-JTAG-TMS	
Pin 15	VCC_3V3	
Pin 16	DEBUG-JTAG-TDO	
Pin 17	GND	
Pin 18	DEBUG-JTAG-TCK	

3.12 Power consumption

Nominally: < 1.5W

Maximum power consumption is dependent on the numbers of interfaces used and the connected equipment.

3.13 Protection

All inputs and outputs of the Sirius OBC have ESD protection. This makes the Sirius OBC robust against unintended damage to the unit through static discharge. Regardless, the units shall only be operated in an ESD safe area.

3.14 Grounding

All Sirius products are designed with separated power/signal ground and chassis ground, connected only capacitively and with a high impedance bleed resistor. When assembled in the spacecraft, the chassis ground shall be bonded to the structure using the grounding point on the case. The grounding point is an M3 threaded hole. If several Sirius units are assembled in a stack configuration, only one of the grounding points need to be used.

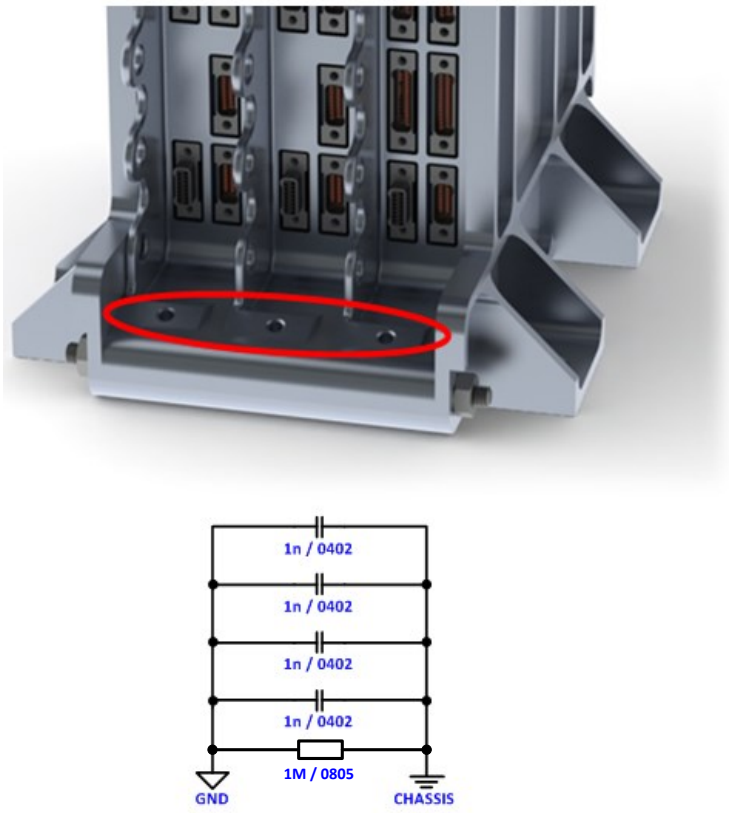


Figure 7 The Sirius products ground and chassis concept

3.14.1 Protection of unused connectors

It is recommended to cover any connectors which are not used in flight. This can be done either through attaching small metal cover plates, or through filling the unused connector with epoxy. The recommended epoxy for this application is 3M Scotchweld 2216. When epoxyfilling the connectors, the Sirius product should be placed in such a way that the connector forms a bathtub, preventing the epoxy from pouring out of the connector during curing.