Sirius OBC – Interface Control Document

H

Revision log

Rev	Date	Change description
A	2017-01-13	Released version
B	2017-10-03	Released version
C	2017-11-28	Released version
D	2018-06-21	Figure 2, mechanical hole dimension added. Clarifications on I/O specifications Added UART5.
E	2019-06-05	Update of SpaceWire connector pinouts
F	2020-11-26	Add information on screws and torques
G	2022-05-04	Reformatting, Added frequency plan and picture of inrush current, SurTec coating possibility added, Updates of interface schematics, Corrections of interface specs, differential GPIO description, frequency plan update
H	2023-06-19	Update grounding section, minor updates

Table of content

1. Introduction

This ICD is written for electrical and mechanical engineers using the AAC CS Sirius products. For software interface descriptions please see the Sirius Product User Manual document [RD1].

1.1. Reference documents

RD#	Document ref	Document name
RD1	205065	Sirius Product User Manual
RD2	104429	OBC-S enclosure drawing

1.2. Acronyms and abbreviations

Acronym	Description
AAC CS	AAC Clyde Space
ADC	Analog to Digital Converter
CoM	Center of Mass
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
ICD	Interface Control Document
MEMS	Microelectromechanical systems
MoI	Moment of Inertia
LVDS	Low-voltage differential signaling
LVTTL	Low-voltage Transistor-Transistor Logic
OBC	On Board Computer
PPS	Pulse Per Second
PSU	Power Supply Unit
SpW	SpaceWire
TBD	To Be Defined
TCM	TT&C Control Module
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter

2. Mechanical ICD

2.1. General

All products in the Sirius AAC CS product family share the same aluminum case. The case is designed to be configured as a stack that fits within the form factor of the CubeSat (PC104) standard. The Sirius OBC step file [RD2] provides a detailed representation of the mechanical form factor.

Figure 2.1 The Sirius OBC product without lid.

2.2. Physical properties

PROPERTY	COMMENT	VALUE
MASS	including top lid	128 g
VOLUME	space occupied by the enclosure	46 cm^3

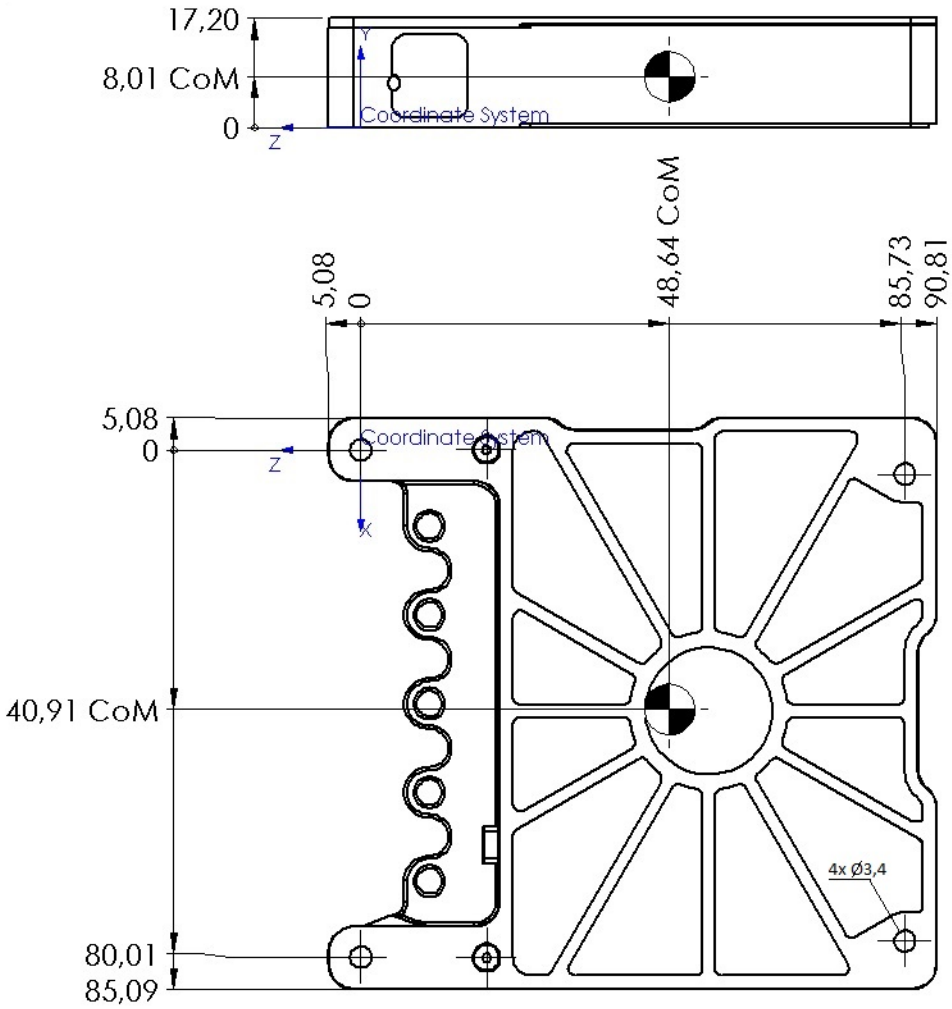


Figure 2.2 The dimensions of the Sirius OBC product, all measurements in mm.

2.3. Center of mass

The center of mass (CoM) is identified in Figure 2.2 with the origin and direction of the coordinate system indicated by the blue text. Numbers are calculated based on SolidWorks CAD model.

AXIS	CENTER OF MASS
X	41 mm
Y	8 mm
Z	−49 mm

2.4. Moment of inertia and other mechanical data

As the Sirius OBC is typically provided in a combined data handling system, mechanical parameters are highly configuration dependent. These are therefore available on request.

2.5. Thermal dissipation

The primary thermal interface area of the unit is the flat surface on the +x face of the unit as shown in Figure 2.2 and marked blue in Figure 2.3. The maximum allowed temperature at the thermal interface is 60 °C, this figure is what has been used for design analysis and exceeding it will violate component derating rules. The size of the thermal interface area is 1 213 mm^2.

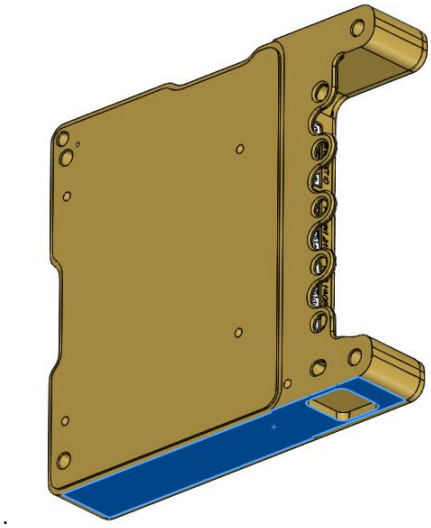


Figure 2.3 The Sirius products thermal interface

To aid in thermal transfer between the Sirius OBC and the surface to which it is mounted, a thermal interface pad is recommended to be placed between Sirius OBC and the spacecraft structure. The recommended TIM is Parker Cho-Therm 1671 or Laird Technology TGON 800. If an electrically insulating material is used, it is necessary to tie the structure to ground using the provided ground bonding point on the enclosure as described in Section 3.3.

2.6. Screws and torques

The debug hatch on the Sirius OBC is held in place with countersunk M2×6, A4-70 screws. The unit is delivered with the debug hatch fitted for transport purposes, but screws are not torqued nor secured for flight. It is the customer's responsibility, as part of system integration process, to torque these screws to 0.25 Nm and apply staking glue when no further access to debug interface is needed. Figure 2.4 shows the location of the debug hatch screws (a DHS including OBC and TCM is shown).

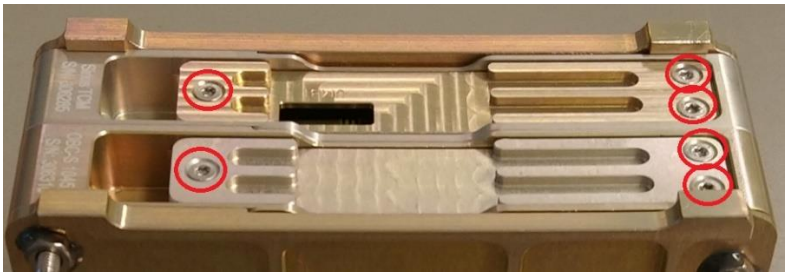


Figure 2.4 Countersunk screws for debug hatch covering the JTAG and Debug connectors.

2.7. Coating

The unit can be surface treated with either Alodine 1200S or SurTec 650, providing corrosion resistance and electrical surface conductivity. The choice of the surface treatment is available to the costumer.

3. Electrical ICD

3.1. Connector locations and pinout

Figure 3.1 illustrates the locations of all connectors on the Sirius OBC.

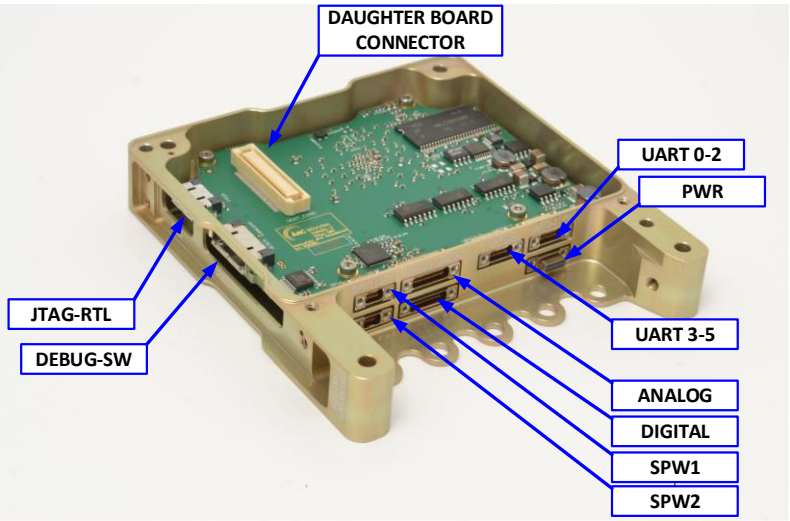


Figure 3.1 The connectors of the Sirius OBC

3.1.1. PWR connector

This connector provides the input power for the unit, as well as PPS transceiver, two RS485 communication interfaces and pulse commands input.

nanoD15 Plug Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	VBUS+	Power input, positive
2	VBUS+	
3	UART7_RXTX_RS485_P	UART7(1) (RS485)
4	UART7_RXTX_RS485_N	
5	PPS_RS422_P	PPS transceiver (in/out)
6	PPS_RS422_N	
7	UART6_RXTX_RS485_P	UART6(2) (RS485)
8	UART6_RXTX_RS485_N	
9	GND	Power return, signal/power ground
10	GND	
11	GND	
12	PULSE0_I_RS422_P	Pulse Command 0
13	PULSE0_I_RS422_N	
14	PULSE1_I_RS422_P	Pulse Command 1
15	PULSE1_I_RS422_N	

Note 1: legacy name "SAFEBUS".
Note 2: legacy name "PSU control".

3.1.2. UART0–2 connector

This connector provides three independent UART interfaces, each configurable to operate either in RS422 or RS485 mode (full- and half-duplex). To configure an interface for RS485 mode operation connect respective UARTx_RX_P pin to UARTx_TX_P and UARTx_RX_N pin to UARTx_TX_N.

nanoD15 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	UART0_RX_P	UART0 receive
2	UART0_RX_N	
3	UART0_TX_P	UART0 transmit
4	UART0_TX_N	
5	GND	Reference potential, signal/power ground
6	GND	
7	UART1_RX_P	UART1 receive
8	UART1_RX_N	
9	UART1_TX_P	UART1 transmit
10	UART1_TX_N	
11	UART2_RX_P	UART2 receive
12	UART2_RX_N	
13	UART2_TX_P	UART2 transmit
14	UART2_TX_N	
15	GND	Reference potential, signal/power ground

3.1.3. UART3–5 connector

This connector provides three independent UART interfaces, each configurable to operate either in RS422 or RS485 mode (full- and half-duplex). To configure an interface for RS485 mode operation connect respective UARTx_RX_P pin to UARTx_TX_P and UARTx_RX_N pin to UARTx_TX_N.

nanoD15 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	UART3_RX_P	UART3 receive
2	UART3_RX_N	
3	UART3_TX_P	UART3 transmit
4	UART3_TX_N	
5	GND	Reference potential, signal/power ground
6	GND	
7	UART4_RX_P	UART4 receive
8	UART4_RX_N	
9	UART4_TX_P	UART4 transmit
10	UART4_TX_N	
11	UART5_RX_P	UART5 receive
12	UART5_RX_N	
13	UART5_TX_P	UART5 transmit
14	UART5_TX_N	
15	GND	Reference potential, signal/power ground

3.1.4. DIGITAL connector

This connector provides several digital I/O interfaces and an external interface for a PPS time synchronization signal.

Each two GPIO signals can be alternatively configured to work in pair as complementary differential outputs. This configuration affects control logic only, signaling levels remain same (LVTTL) in both single and differential mode.

nanoD25 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	GPIO 0	LVTTL digital input/output
2	GPIO 1	LVTTL digital input/output, *alt. configuration: complementary LVTTL output to GPIO0*
3	GPIO 2	LVTTL digital input/output
4	GPIO 3	LVTTL digital input/output, *alt. configuration: complementary LVTTL output to GPIO2*
5	GPIO 4	LVTTL digital input/output
6	GPIO 5	LVTTL digital input/output, *alt. configuration: complementary LVTTL output to GPIO4*
7	GPIO 6	LVTTL digital input/output
8	GPIO 7	LVTTL digital input/output, *alt. configuration: complementary LVTTL output to GPIO6*
9	GPIO 8	LVTTL digital input/output
10	GPIO 9	LVTTL digital input/output, *alt. configuration: complementary LVTTL output to GPIO8*
11	GPIO 10	LVTTL digital inputs/outputs with internal 10 kΩ pull-up
12	GPIO 11	LVTTL digital inputs/outputs with internal 10 kΩ pull-up, *alt. configuration: complementary LVTTL output to GPIO10*
13	GND	Reference potential, signal/power ground
14	*Reserved*	Do not connect
15	*Reserved*	
16	*Reserved*	
17	*Reserved*	
18	*Reserved*	
19	*Reserved*	
20	*Reserved*	
21	*Reserved*	
22	*Reserved*	
23	PPS_IN_ N	Differential PPS input for time synchronization
24	PPS_IN_ P	
25	GND	Reference potential, signal/power ground

3.1.5. ANALOG connector

This connector provides 10 analog input channels, reference voltage output and several digital IOs.

nanoD25 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	ADC_IN_0	Analog input to ADC
2	ADC_IN_1	Analog input to ADC
3	ADC_IN_2	Analog input to ADC
4	ADC_IN_3	Analog input to ADC
5	ADC_IN_4	Analog input to ADC
6	ADC_IN_5	Analog input to ADC
7	ADC_IN_6	Analog input to ADC
8	ADC_IN_7	Analog input to ADC
9	V_REF	Buffered 2.5V reference for ADC measurements
10	V_REF	
11	GPIO12	LVTTL digital input/output
12	GPIO13	LVTTL digital input/output, *alt. configuration: complementary LVTTL output to GPIO12*
13	GPIO14	LVTTL digital input/output
14	GND	Reference potential, signal/power ground
15	GND	
16	GND	
17	GND	
18	GND	
19	GND	
20	GND	
21	GND	
22	V_REF	Buffered 2.5V reference for ADC measurements
23	V_REF	
24	GPIO15	LVTTL digital input/output, *alt. configuration: complementary LVTTL output to GPIO14*
25	GND	Reference potential, signal/power ground

3.1.6. SPW1 connector

The connector provides one SpaceWire communication interfaces with standard pinout.

nanoD9 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	SPW1_DIN_LVDS_P	Data in, Positive
2	SPW1_SIN_LVDS_P	Strobe in, Positive
3	GND(1)	Reference potential, signal/power ground(1)
4	SPW1_SOUT_LVDS_N	Strobe out, Negative
5	SPW1_DOUT_LVDS_N	Data out, Negative
6	SPW1_DIN_LVDS_N	Data in, Negative
7	SPW1_SIN_LVDS_N	Strobe in, Negative
8	SPW1_SOUT_LVDS_P	Strobe out, Positive
9	SPW1_DOUT_LVDS_P	Data out, Positive

Note 1: Older hardware revisions can have pin 3 not connected or connected to chassis.

3.1.7. SPW2 connector

The connector provides one SpaceWire communication interfaces with standard pinout.

nanoD9 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	SPW2_DIN_LVDS_P	Data in, Positive
2	SPW2_SIN_LVDS_P	Strobe in, Positive
3	GND(1)	Reference potential, signal/power ground(1)
4	SPW2_SOUT_LVDS_N	Strobe out, Negative
5	SPW2_DOUT_LVDS_N	Data out, Negative
6	SPW2_DIN_LVDS_N	Data in, Negative
7	SPW2_SIN_LVDS_N	Strobe in, Negative
8	SPW2_SOUT_LVDS_P	Strobe out, Positive
9	SPW2_DOUT_LVDS_P	Data out, Positive

Note 1: Older hardware revisions can have pin 3 not connected or connected to chassis.

3.1.8. DEBUG-SW connector

This connector provides the programming interface for the AAC Clyde Space debugger.

ST60-18P connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	ETH-DEBUG-RESET	Interface to AAC Clyde Space debugger
2	ETH-DEBUG-DETECT	
3	ETH-DEBUG-SYNC	
4	ETH-DEBUG-TX	
5	ETH-DEBUG-RX	
6	ETH-DEBUG-MDC	
7	ETH-DEBUG-MDIO	
8	ETH-DEBUG-CLK	
9	GND	
10	DEBUG-JTAG-TDI	
11	DEBUG-JTAG-RX	
12	DEBUG-JTAG-TX	
13	VCC_3V3	
14	DEBUG-JTAG-TMS	
15	VCC_3V3	
16	DEBUG-JTAG-TDO	
17	GND	
18	DEBUG-JTAG-TCK	

3.1.9. JTAG-RTL connector

This connector provides an interface to program the FPGA during manufacturing.

ST60-10P connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
1	GND	Interface to Microsemi FlashPro programmer
2	RTL-JTAG-TDI	
3	RTL-JTAG-TRSTB	
4	VCC_3V3	
5	VCC_3V3	
6	RTL-JTAG-TMS	
7	Not connected	
8	RTL-JTAG-TDO	
9	GND	
10	RTL-JTAG-TCK	

3.1.10. Daughter board connector

The Sirius OBC has a Hirose FX8C 60-pin board-to-board connector allowing daughter boards to be fitted to the unit. No signals are present on this connector by default, but AAC CS can upon request develop customer specific add-ons using this interface.

3.2. Interface specification and diagrams

3.2.1. Power input

Sirius OBC internal ground and reference voltage for all interface signals is galvanically connected to ground.

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
INPUT VOLTAGE	between VBUS+ and GND	4.5		16	V
POWER-ON THRESHOLD			4.4		V
UNDERVOLTAGE PROTECTION HYSTERESIS			0.4		V
INPUT POWER	idle(1), 4.5 V in idle(1), 16 V in		1.2 1.6		W W
GROUND TO CHASSIS POTENTIAL	Note 2	−5	0	+5	V

Note 1: Power consumption is measured during acceptance testing with minimal housekeeping code running and without any connected peripherals. Actual value in specific application depends on the number of interfaces used, connected equipment and system load.

Note 2: Low voltage ground is assumed to nominally be at 0 V w.r.t chassis/structure.

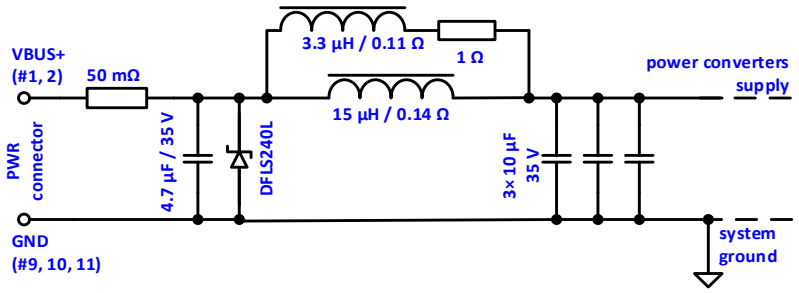


Figure 3.2 shows the inrush current waveform when powered from a Class 0.5 LCL.

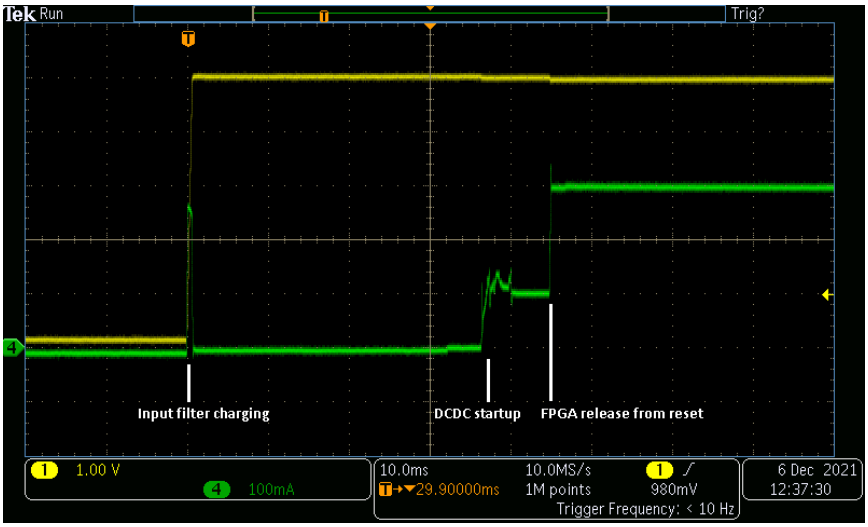


Figure 3.2 Inrush current waveform when powered from Class 0.5 LCL, Yellow=input voltage, Green=input current

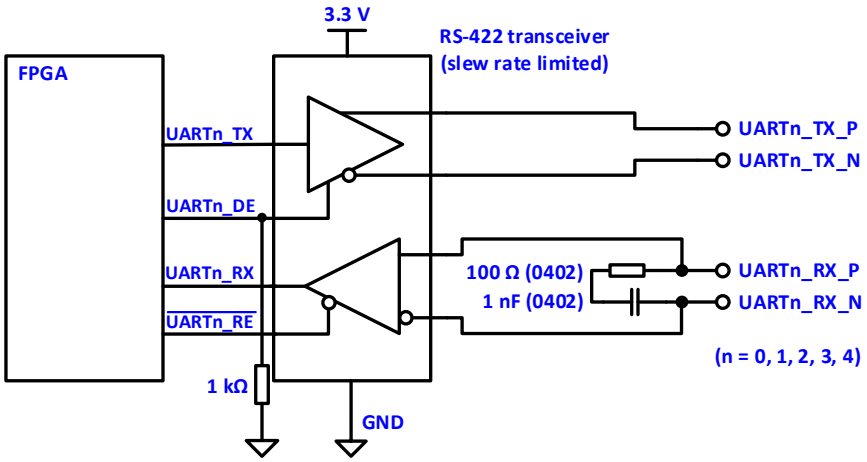
3.2.2. UART0 to UART4 (RS-422/RS-485)

The standard operating mode of UART0 to UART4 interfaces is RS-422, but any of them can be reconfigured in half-duplex RS-485 mode.

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
SIGNALING RATE		1.2		375	kBaud
TX					
DIFFERENTIAL OUTPUT VOLTAGE	100 Ω termination	2.0		3.3	V
	54 Ω termination	1.5		3.3	V
COMMON MODE OUTPUT VOLTAGE	relative to power return		1.65		V
SINGLE-ENDED OUTPUT VOLTAGE	relative to power return	0		3.3	V
OUTPUT RISE/FALL TIME	54 Ω and 50 pF load	0.2		0.8	µs
TRANSMITTER LOAD	total termination impedance(2)	50			Ω
RX					
INPUT DIFFERENTIAL THRESHOLD	between logic 0 and 1	−200	−125	−50	mV
ALLOWED DIFFERENTIAL VOLTAGE		−6		+6	V
ALLOWED INPUT, EACH SINGLE PIN	relative to power return	−7		+12	V

Note 1: Logic 1 signal is defined as pin "_P" positive relative to respective pin "_N". Open or short circuit on receiver pins results in logic 1 being detected.

Note 2: When used in RS485 mode, the internal AC termination needs to be taken into account when computing total terminator load.



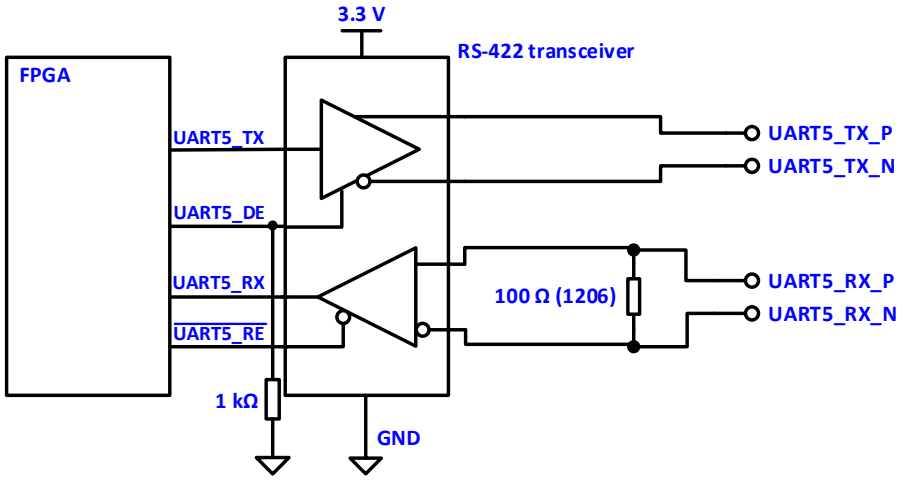
3.2.3. UART5 (RS-422/RS-485)

The UART5 interface standard operating mode is RS-422, but it can be reconfigured in half-duplex RS-485 mode.

Caution: This interface does not support full RS-422 differential voltage range. Maximum allowed differential voltage applied to RX pins is +/− 3.5 V.

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
SIGNALING RATE		1.2		375[2]	kBaud
TX					
DIFFERENTIAL OUTPUT VOLTAGE	100 Ω termination	2.0		3.3	V
	54 Ω termination	1.5		3.3	V
COMMON MODE OUTPUT VOLTAGE	relative to power return		1.65		V
SINGLE-ENDED OUTPUT VOLTAGE	relative to power return	0		3.3	V
OUTPUT RISE/FALL TIME	54 Ω and 50 pF load			15	ns
TRANSMITTER LOAD	total termination impedance[3]	50			Ω
RX					
INPUT DIFFERENTIAL THRESHOLD	between logic 0 and 1	−200	−125	−50	mV
ALLOWED DIFFERENTIAL VOLTAGE		−3.5		+3.5	V
ALLOWED INPUT, EACH SINGLE PIN	relative to power return	−7		+12	V

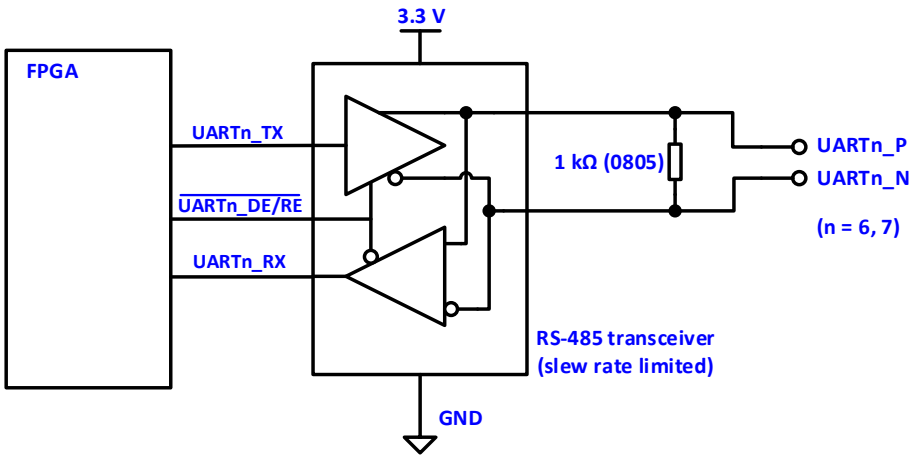
Note 1: Logic 1 signal is defined as pin "_P" positive relative to respective pin "_N". Open or short circuit on receiver pins results in logic 1 being detected.
Note 2: Limited by current software/firmware capabilities.
Note 3: The internal 100 Ω termination needs to be accounted for when computing total load in RS-485 mode.



3.2.4. UART6 and UART7 (RS-485)

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
SIGNALING RATE		1.2		375	kBaud
DIFFERENTIAL OUTPUT VOLTAGE	100 Ω termination	2.0		3.3	V
	54 Ω termination	1.5		3.3	V
COMMON MODE OUTPUT VOLTAGE	relative to power return		1.65		V
SINGLE-ENDED OUTPUT VOLTAGE	relative to power return	0		3.3	V
OUTPUT RISE/FALL TIME	54 Ω and 50 pF load	0.2		0.8	µs
TRANSMITTER LOAD	total termination impedance	50			Ω
INPUT DIFFERENTIAL THRESHOLD	between logic 0 and 1	−200	−125	−50	mV
ALLOWED INPUT DIFFERENTIAL VOLTAGE		−6		+6	V
ALLOWED VOLTAGE, EACH SINGLE PIN	relative to power return	−7		+12	V

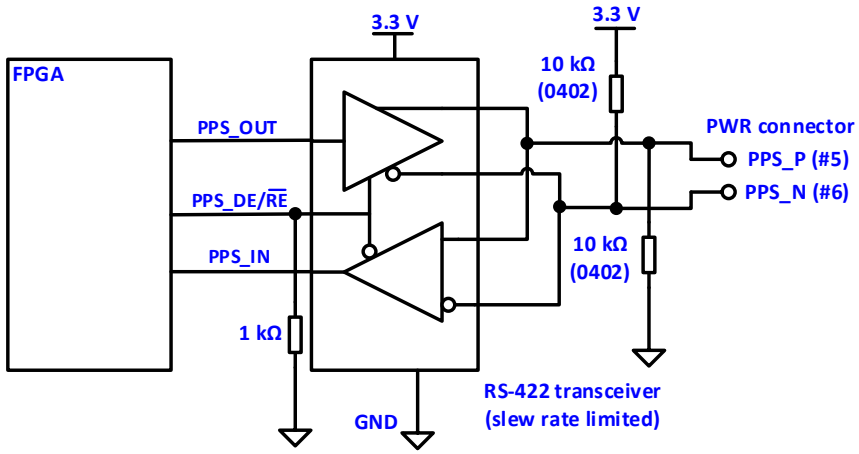
Note 1: Logic 1 signal is defined as pin "_P" positive relative to respective pin "_N". In RX mode, an open or short circuit condition results in logic 1 being detected.



3.2.5. PPS transceiver

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
DIFFERENTIAL OUTPUT VOLTAGE	100 Ω termination	2.0		3.3	V
	54 Ω termination	1.5		3.3	V
COMMON MODE OUTPUT VOLTAGE	relative to power return		1.65		V
SINGLE-ENDED OUTPUT VOLTAGE	relative to power return	0		3.3	V
OUTPUT RISE/FALL TIME	54 Ω and 50 pF load	0.2		0.8	µs
TRANSMITTER LOAD	total termination impedance	50			Ω
PULSE DETECTION DIFFERENTIAL THRESHOLD		−200	−125	−50	mV
ALLOWED INPUT DIFFERENTIAL VOLTAGE		−6		+6	V
ALLOWED VOLTAGE, EACH SINGLE PIN	relative to power return	−7		+12	V
INPUT PPS PULSE LENGTH	required for accepted PPS	1		1000	µs

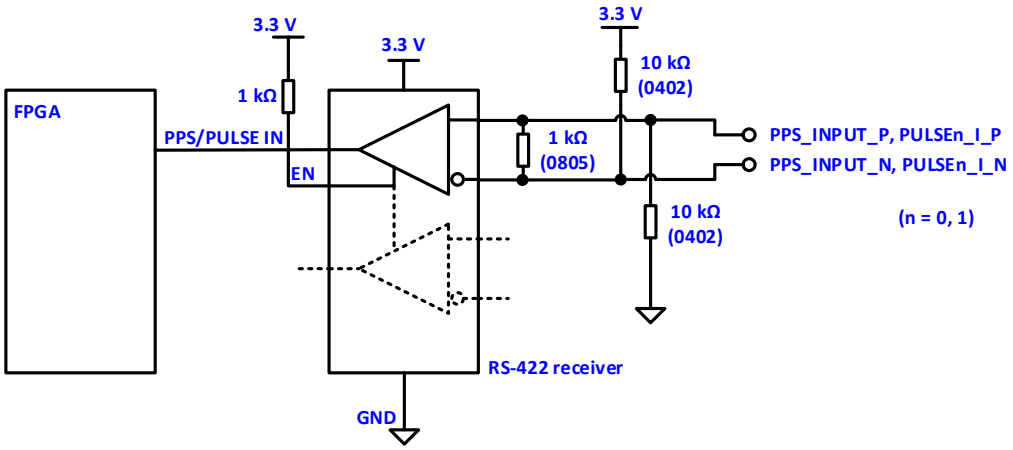
Note 1: Pulse is active when pin "PPS_P" is positive relative to pin "PPS_N".



3.2.6. PPS input and pulse command input

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
PULSE DETECTION DIFFERENTIAL THRESHOLD		−200		+200	mV
ALLOWED INPUT DIFFERENTIAL VOLTAGE		−7		+7	V
ALLOWED VOLTAGE, EACH SINGLE PIN	relative to power return	−7		+7	V
VALID PULSE DURATION	PULSE0 and PULSE1	20		40	ms
	PPS input	1		1000	µs

Note 1: Pulse is detected as active when pin "_P" is positive relative to respective pin "_N".

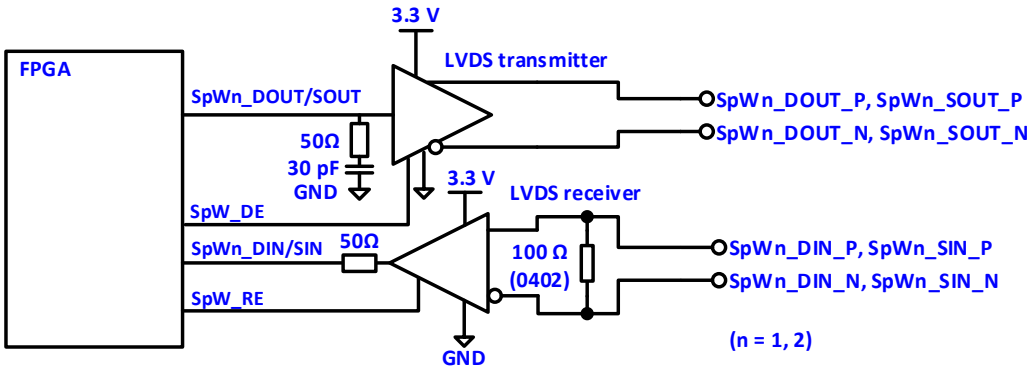


3.2.7. SpaceWire interfaces

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
DATA RATE	After handshake(1)		50		Mbit
TX					
DIFFERENTIAL OUTPUT VOLTAGE	100 Ω load	250	350	450	mV
COMMON MODE OUTPUT VOLTAGE	100 Ω load, relative to GND		1.25		V
SINGLE-ENDED OUTPUT VOLTAGE	100 Ω load, relative to GND	0.9		1.6	V
OUTPUT RISE/FALL TIME	100 Ω and 10 pF load		0.4	1.5	ns
SHORT-CIRCUIT OUTPUT CURRENT				9	mA
REQUIRED TERMINATION	external resistor	90		130	Ω
RX					
INPUT DIFFERENTIAL THRESHOLD	between logic 0 and 1	−100	±20	+100	mV
NOMINAL COMMON MODE VOLTAGE	for 200 mV differential(2)	0.1		2.3	V
ALLOWED DIFFERENTIAL VOLTAGE		−1.5		+1.5	V
ALLOWED INPUT VOLTAGE	single-ended, relative to system GND	0		3.0	V

Note 1: Handshake is performed at 10 Mbit, only 50 Mbit is supported elsewhere

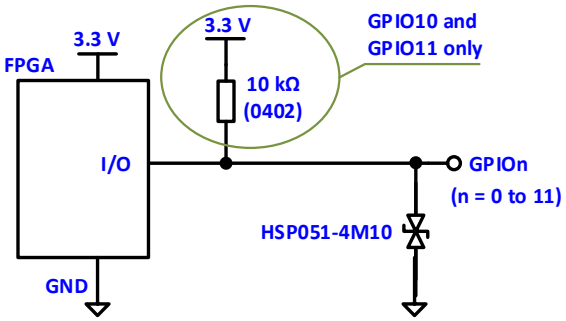
Note 2: For higher differential voltage, narrow the range by V_{ID}/2 at each end.



3.2.8. GPIO interface

PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
OUTPUT					
OUTPUT VOLTAGE, LOW	sinking ≤ 12 mA	0		0.4	V
OUTPUT VOLTAGE, HIGH	sourcing ≤ 12 mA	2.4		3.3	V
OUTPUT CURRENT	do not exceed this value	−12		+12	mA
INPUT					
LOGIC LOW		0		0.8	V
LOGIC HIGH		2.0		3.3	V

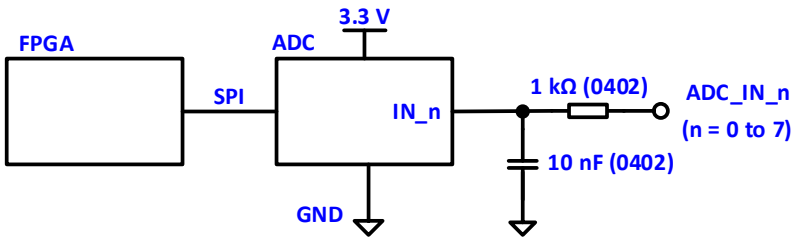
Note 1: All voltages are relative to system GND (power return potential).



3.2.9. Analog input interface

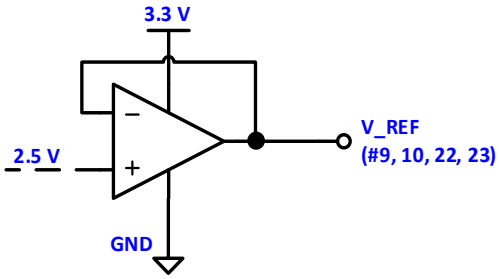
PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
ALLOWED APPLIED INPUT VOLTAGE	relative to system GND	0		3.3	V
ADC OPERATING RANGE	relative to system GND	0		2.1(1)	V
ADC FULL-SCALE VOLTAGE		2.49	2.50	2.51	V
INPUT LEAKAGE CURRENT			±2		nA

Note 1: Up to 3.3 V can be applied at input pin without overstressing the device, but valid conversion result will be obtained for input voltages lower than 2.1 V only.



3.2.10. Voltage reference

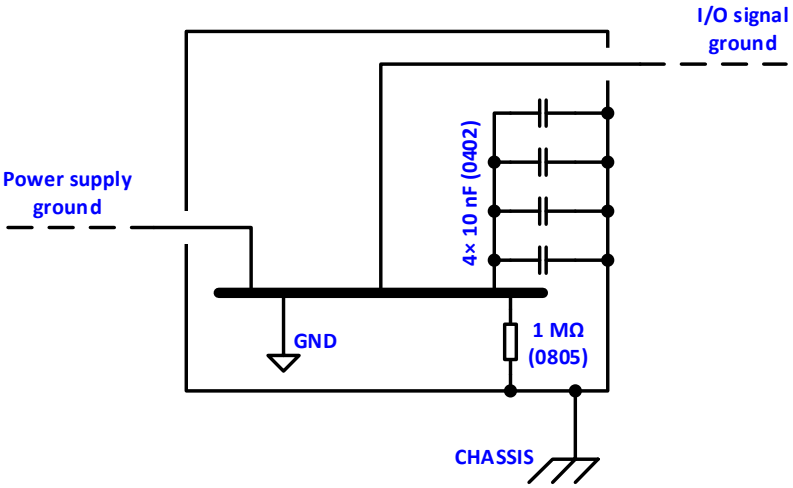
PARAMETER	CONDITIONS/COMMENT	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE	relative to system GND	2.48		2.52	V
OUTPUT CURRENT	positive current is from V_REF to GND	−10		+3	mA
CAPACITIVE LOAD	connected directly to the output			200	pF



3.3. Grounding

Sirius OBC internal power supply converters are not isolated, and the internal unit ground is therefore galvanically connected to power supply return potential. This ground potential forms a reference voltage for all unit electrical interfaces.

Chassis is connected to the internal ground mainly capacitively with a high impedance bleed resistor. Please note that older hardware revisions may have a capacitance of 4x1nF.



When assembled in the spacecraft, the chassis shall be bonded to the spacecraft structure. This is accomplished either through using the grounding point on the case, or through ensuring a low impedance surface-to-surface contact between DHS and spacecraft structure. The grounding point is an M3 threaded hole. If several Sirius units are assembled in a stack configuration, it is sufficient to use only one of the grounding points as the enclosures are electrically connected through mechanical interlocks.

3.4. Fault voltage emission

The worst fault voltage which can be emitted from OBC on any interface is the incoming supply voltage.

3.5. Frequency plan

The frequencies in use for the different interfaces are given in the table below. All clocks are generated from the 100 MHz reference oscillator through division making all clocks synchronous, except when labelled asynchronous in the list below.

Principal frequency [MHz]	Use / Description	Source
100.0	Main system clock	MEMS oscillator
100.0	SDRAM, single data-rate	MEMS oscillator, FPGA
50.0	CPU clock	MEMS oscillator, divided down in FPGA
50.0	SpaceWire #1 and #2, link connected	MEMS oscillator, divided down in FPGA
25.0	System flash data interface	MEMS oscillator, divided down in FPGA
1.0 to 25.0	NVRAM, internal SPI bus	MEMS oscillator, software-configurable division in FPGA
0.20 to 25.0	ADC internal SPI bus	MEMS oscillator, software-configurable division in FPGA
10.0	SpaceWire #1 and #2, link disconnected	MEMS oscillator, divided down in FPGA
3.125	NVRAM, internal SPI bus during boot	MEMS oscillator, divided down in FPGA
0.50 ± 0.12	3.3V DC-DC converter	asynchronous, free running RC-oscillator
0.29 ± 0.07	1.2V DC-DC converter	asynchronous, free running RC-oscillator
≤ 0.375	UART0 to UART7	MEMS oscillator, software-configurable division in FPGA
0.115	debug UART	MEMS oscillator, divided down in FPGA
≤ 0.016	ADC inputs sampling rate	MEMS oscillator, software-configurable division in FPGA