ICD - Sirius OBC

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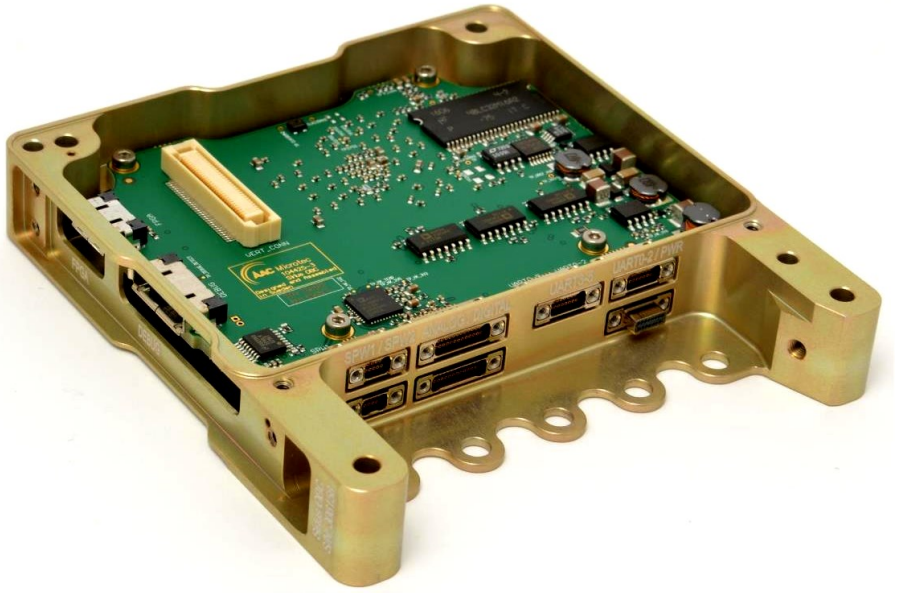


REVISION LOG

Rev	Date	Change description
A	2017-01-13	Released version
B	2017-10-03	Released version
C	2017-11-28	Released version
D	2018-06-21	Released version D with the following updates: - Figure 2, mechanical hole dimension added - Clarifications on I/O specifications - Added UART5
E	2019-06-05	Update of SpaceWire connector pinouts
F	2020-11-26	Add information on screws and torques

TABLE OF CONTENT

1 Introduction

This ICD is written for electrical and mechanical engineers using the ÅAC Sirius products. For software interface descriptions please see the Sirius Product User Manual document [RD1].

1.1 Reference documents

RD#	Document ref	Document name
RD1	205065	Sirius Product User Manual
RD2	104437	OBC-S Product step file

1.2 Acronyms and abbreviations

Acronym	Description
ADC	Analog to Digital Converter
CoM	Center of Mass
ESD	Electro Static Discharge
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit communication
ICD	Interface Control Document
MoI	Moment of Inertia
LVDS	Low-voltage differential signaling
OBC	On Board Computer
PPS	Pulse Per Second
PSU	Power Supply Unit
SPI	Serial Peripheral Interface
SpW	SpaceWire
TBD	To Be Defined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter

2 Mechanical ICD

2.1 General

All products in the Sirius product family share the same aluminum case. The case is designed to be configured as a stack that fits within the form factor of the CubeSat (PC104) standard. The Sirius OBC step file [RD2] provides a detailed representation of the mechanical form factor.

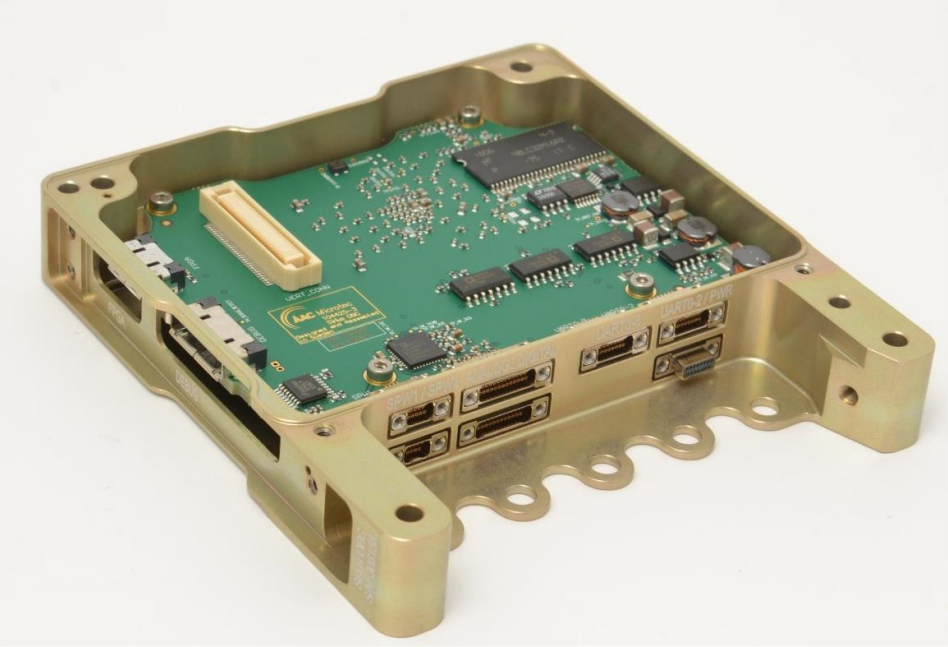


Figure 1 - The Sirius OBC product without lid

2.2 Physical properties

Property	Value	Units
Mass	127.85	gram
Volume	46315	mm^3
Surface area	69879	mm^2

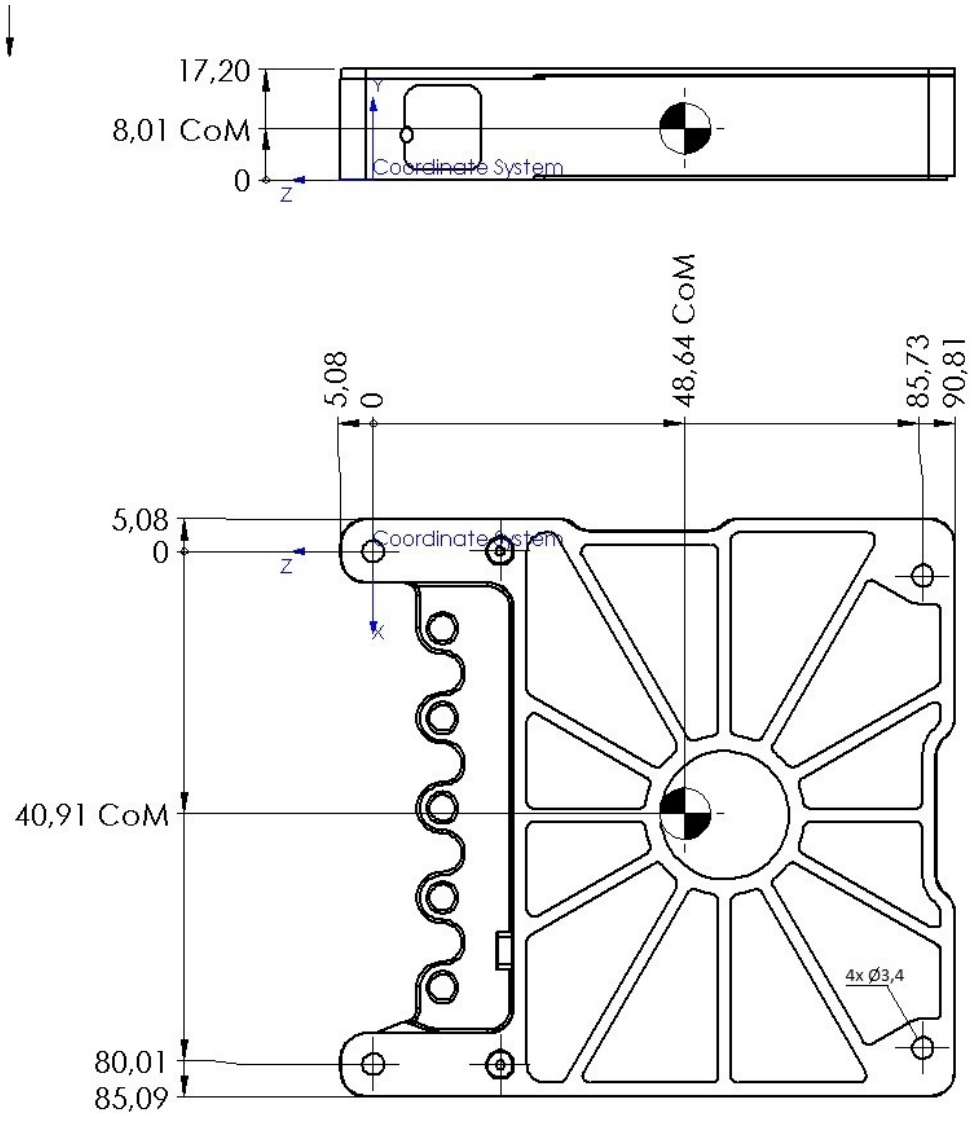


Figure 2 - The dimensions of the Sirius OBC product, all measurements in mm

2.3 Center of Mass

The center of mass (CoM) is identified in Figure 2 with the origin and direction of the coordinate system indicated by the blue text.

AXIS	Center Of Mass [mm]
X	40.91
Y	8.01
Z	-48.64

2.4 Moment of inertia

The moment of inertia (MoI) for the mechanical structure is defined by the table below using the coordinate system origin is defined by Figure 2.

MOMENTS OF INERTIA [g*mm²]					
Principal axes of inertia and principal moments of inertia taken at the center of mass.		Taken at the center of mass and aligned with the output coordinate system.		Taken at the output coordinate system.	
Ix	(0.99, 0.00, 0.17)	**Lxx**	97222	**Ixx**	407860
Iy	(0.17, 0.00, -0.99)	**Lyx**	-5	**Iyx**	41876
Iz	(0.00, 1.00, 0.00)	**Lzx**	3263	**Izx**	-251131
Px	96666	**Lxy**	-5	**Ixy**	41876
Py	116367	**Lyy**	205817	**Iyy**	722241
Pz	205818	**Lzy**	-180	**Izy**	-49971
		Lxz	3263	**Ixz**	-251131
		Lyz	-180	**Iyz**	-49971
		Lzz	115811	**Izz**	337991

2.5 Mechanical resonance frequencies

Mode	Frequency [Hz]
1	563.55
2	681.58
3	876.37
4	1231.9
5	1355.8

2.6 Thermal dissipation

The primary thermal interface area of the unit is the flat surface on the +x face of the unit as shown in Figure 2 and marked blue in Figure 3. The maximum allowed temperature at the thermal interface is 60°C, this figure is what has been used for design analysis and exceeding it will violate component derating rules. The size of the thermal interface area is 1212.75 mm^2.

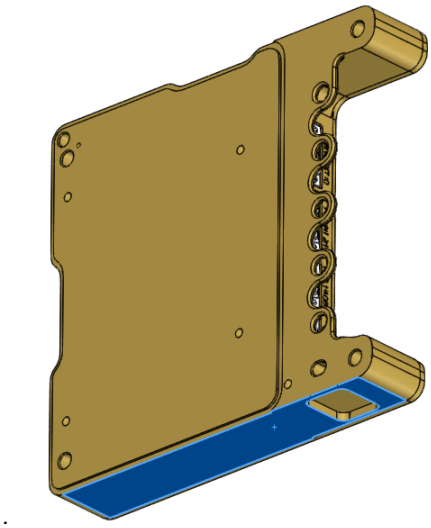


Figure 3 - The Sirius products thermal interface

To aid in thermal transfer between the Sirius OBC and the surface to which it is mounted, a thermal interface pad is recommended to be placed between Sirius OBC and the spacecraft structure. The recommended TIM is Parker Cho-Therm 1671.

2.7 Screws and torques

The lid and debug hatch on the Sirius OBC are held in place with countersunk M2x6 A4-70 screws, two for the lid and three for the debug hatch. All screws shall be torqued to 0.25 Nm.

2.8 Coating

The unit is surface treated with Alodine 1200S providing corrosion resistance and electrical surface conductivity. Surfaces have an emissivity (ε) of 0.068 and absorptivity (α) of 0.15.

3 Electrical ICD

Figure 4 illustrates the locations of all connectors on the Sirius OBC.

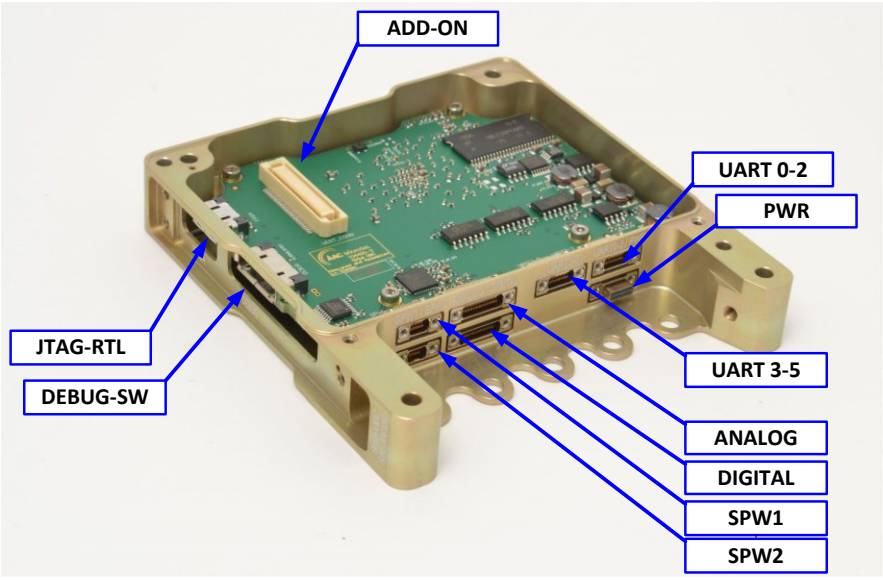


Figure 4 - The connectors of the Sirius OBC

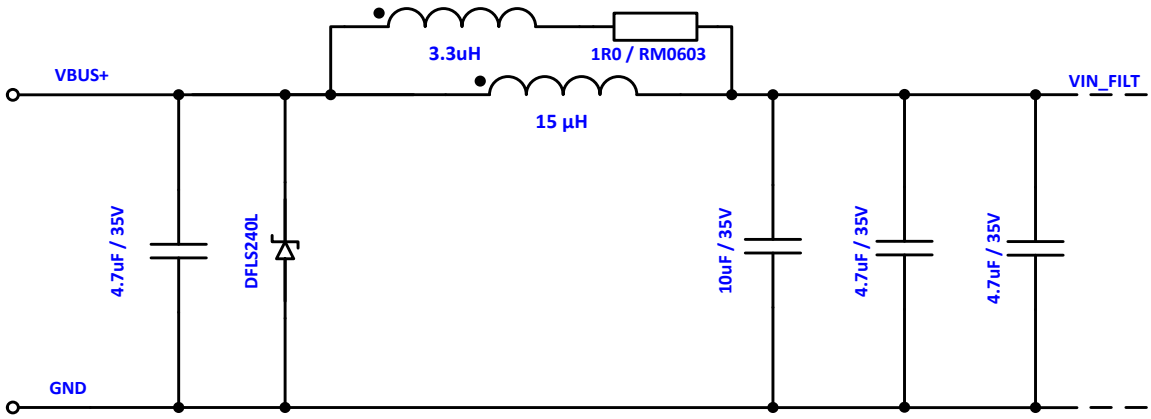
Note: The RS422 and RS485 interfaces define the P/N signals as a one (1) if P is positive and N is negative.

3.1 PWR connector

This connector provides the input power for the unit, as well as PPS transceiver, pulse commands and safe mode communication interfaces.

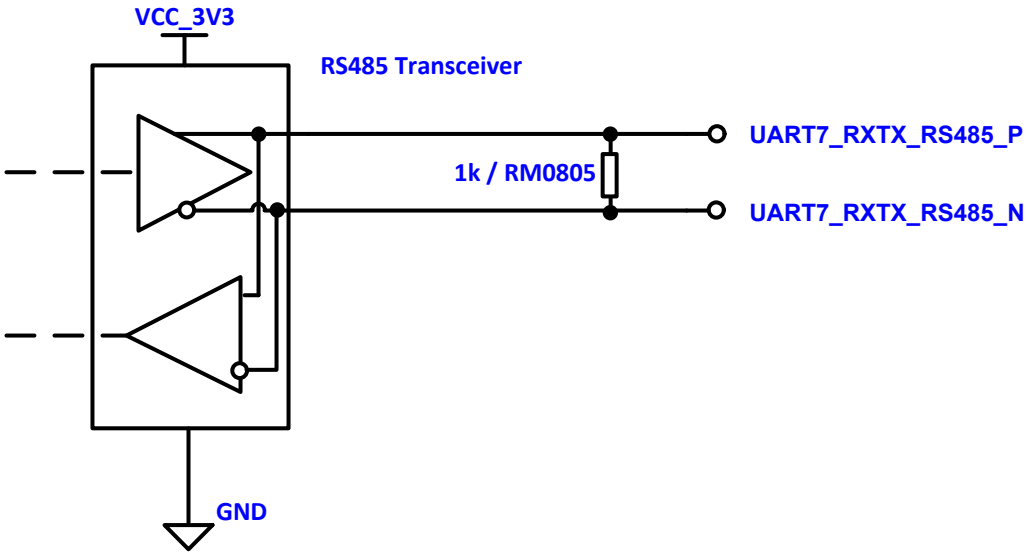
nanoD15 Plug Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	VBUS+	Power input
Pin 2	VBUS+	
Pin 3	UART7_RXTX_RS485_P	UART7 (SAFEBUS, RS485)
Pin 4	UART7_RXTX_RS485_N	
Pin 5	PPS_RS422_P	PPS transceiver
Pin 6	PPS_RS422_N	
Pin 7	UART6_RXTX_RS485_P	UART6 (PSU control, RS485)
Pin 8	UART6_RXTX_RS485_N	
Pin 9	GND	Ground
Pin 10	GND	
Pin 11	GND	
Pin 12	PULSE0_I_RS422_P	Pulse Command 0
Pin 13	PULSE0_I_RS422_N	
Pin 14	PULSE1_I_RS422_P	Pulse Command 1
Pin 15	PULSE1_I_RS422_N	

3.1.1 VBUS - Power Input



NAME	DESCRIPTION	CONNECTOR PINS	VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [A]	MAX [A]
VBUS+	Power input	1, 2	+4.5	+16.0	0	0.6
GND	Power return	9, 10, 11	0	0.1	0	0.6

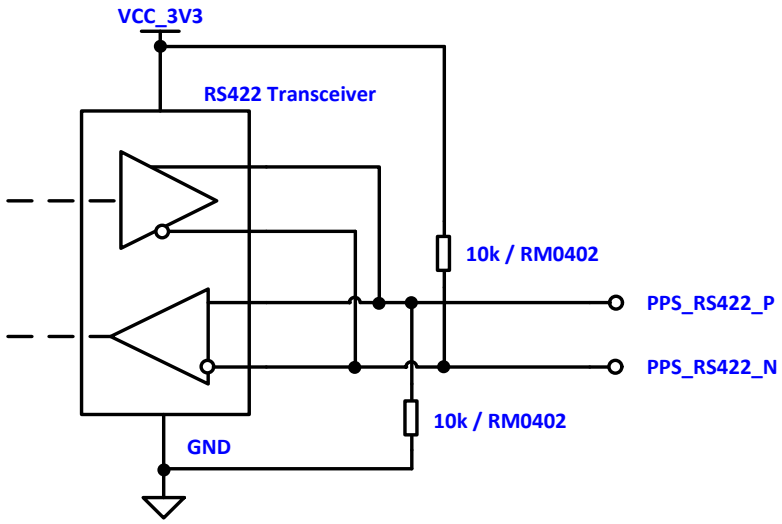
3.1.2 UART7 – SAFEBUS



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART7_RXTX_RS485_P	SAFEBUS Output mode	3	2.0	0	0.4	2.4	3.6	-20	+20
UART7_RXTX_RS485_N		4		0	0.4	2.4	3.6	-20	+20
UART7_RXTX_RS485_P	SAFEBUS Input mode	3	0.2	-7	-	-	+12	-3.6	+3.6
UART7_RXTX_RS485_N		4		-7	-	-	+12	-3.6	+3.6

3.1.3 PPS transceiver

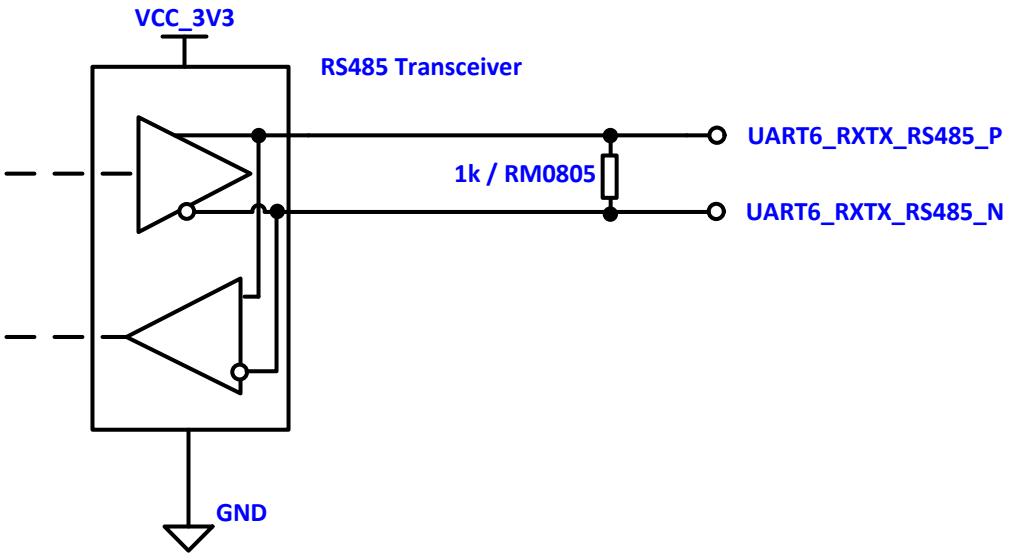
To provide external time synchronization, a PPS input-only is provided as defined in section 3.6.2. This PPS transceiver can act as both a distributor and receiver of the PPS, configurable by SW.



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
PPS_RS422_P	PPS Output mode	5	2.0	0	+0.4	+2.4	+3.6	-20	+20
PPS_RS422_N		6		0	+0.4	+2.4	+3.6	-20	+20
PPS_RS422_P	PPS Input mode	5	0.2	-7	-	-	+12	-3.6	+3.6
PPS_RS422_N		6		-7	-	-	+12	-3.6	+3.6

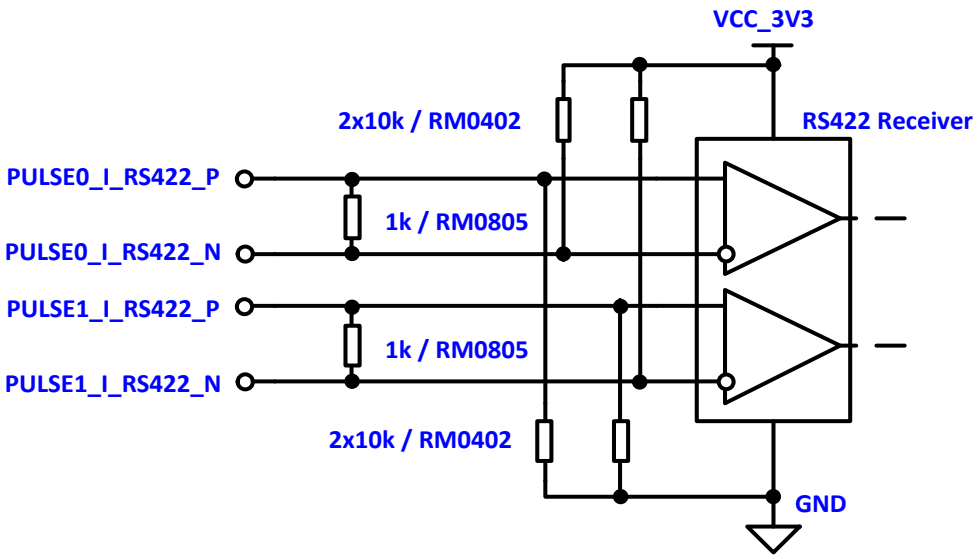
Note: The PPS pulse shall be within 1 us – 1 ms time window with differential RS422 voltage levels. A valid PPS pulse shall be logic high.

3.1.4 UART6 - PSU Control



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART6_RXTX_RS485_P	PSU CTRL Output mode	7	2.0	0	0.4	2.4	3.6	-20	+20
UART6_RXTX_RS485_N		8		0	0.4	2.4	3.6	-20	+20
UART6_RXTX_RS485_P	PSU CTRL Input mode	7	0.2	-7	-	-	+12	-3.6	+3.6
UART6_RXTX_RS485_N		8		-7	-	-	+12	-3.6	+3.6

3.1.5 PULSE command input



NAME	DESCRIPTION	PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]
PULSE0_I_RS422_P	Pulse Command Input	12	0.2	-7	-	-	+7
PULSE0_I_RS422_N		13		-7	-	-	+7
PULSE1_I_RS422_P	Pulse Command Input	14	0.2	-7	-	-	+7
PULSE1_I_RS422_N		15		-7	-	-	+7

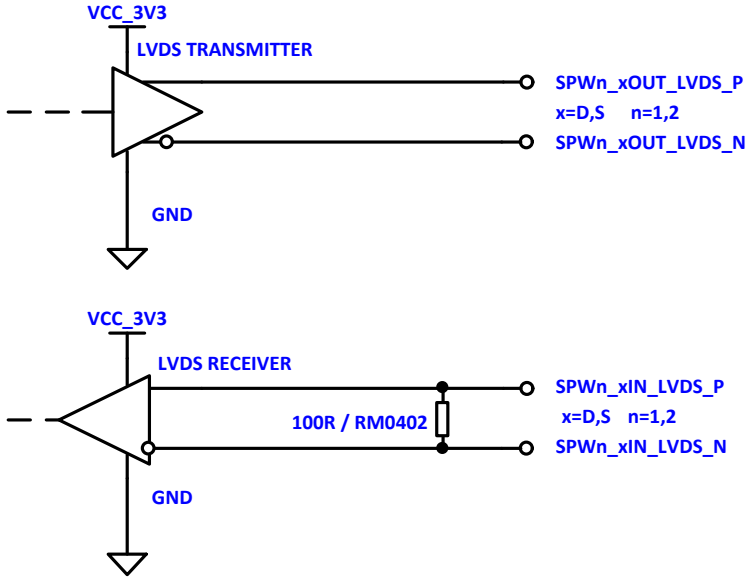
Note: A valid pulse command shall have a minimum length of 20 ms and a maximum length of 40 ms. The pulse shall have differential RS422 levels. A valid pulse command shall have both a rising edge and a falling edge, in that order.

3.2 SPW1 connector

This connector has one of the two SpaceWire communication interfaces.

nanoD9 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	SPW1_DIN_LVDS_P	Data in, Positive
Pin 2	SPW1_SIN_LVDS_P	Strobe in, Positive
Pin 3	CGND[1]	Chassis ground[1]
Pin 4	SPW1_SOUT_LVDS_N	Strobe out, Negative
Pin 5	SPW1_DOUT_LVDS_N	Data out, Negative
Pin 6	SPW1_DIN_LVDS_N	Data in, Negative
Pin 7	SPW1_SIN_LVDS_N	Strobe in, Negative
Pin 8	SPW1_SOUT_LVDS_P	Strobe out, Positive
Pin 9	SPW1_DOUT_LVDS_P	Data out, Positive

Note 1: Pin 3 can be connected to CGND or NC, depending on hardware configuration. Both have equivalent EMI and signal integrity performance.



NAME	DESCRIPTION	CONNECTOR PINS	DIFF. VOLTAGE		LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
SPW1_DIN_LVDS_P	Data in	1	0.1	1.8	0	-	-	3.3	-17	17
SPW1_DIN_LVDS_N		6			0	-	-	3.3	-17	17
SPW1_SIN_LVDS_P	Strobe in	2	0.1	1.8	0	-	-	3.3	-17	17
SPW1_SIN_LVDS_N		7			0	-	-	3.3	-17	17
SPW1_DOUT_LVDS_P	Data out	9	0.25		0.9	-	-	1.6	-6.0	6.0
SPW1_DOUT_LVDS_N		5			0.9	-	-	1.6	-6.0	6.0
SPW1_SOUT_LVDS_P	Strobe out	8	0.25		0.9	-	-	1.6	-6.0	6.0
SPW1_SOUT_LVDS_N		4			0.9	-	-	1.6	-6.0	6.0

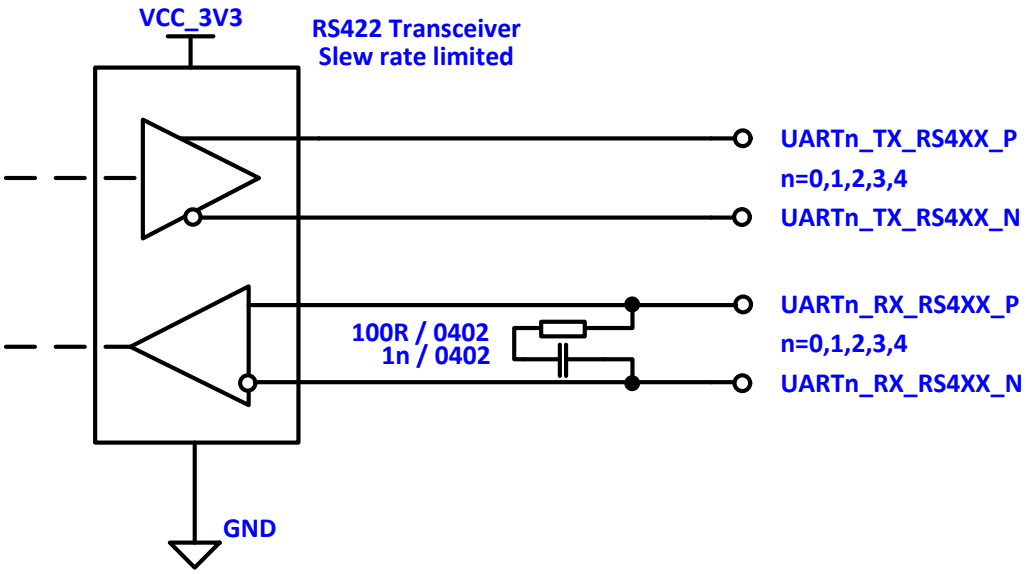
3.3 SPW2 connector

The SPW2 – SpaceWire signal names and signal behavior are the same as described in section 3.2. Signal index names are changed from SPW1 to SPW2. The electrical interface schematics are identical to those shown in section 3.2.

3.4 UART 0-2 connector

This connector provides three RS422 UART interfaces that can also be used in RS485 configuration through connecting input and output circuits to one signal pair. The RS422/485 UARTs support up to 400 kBaud signaling rate before violating the power derating for the termination resistor.

nanoD15 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	UART0_RX_RS4XX_P	UART0 RX. For RS485 mode, connect to UART0 TX
Pin 2	UART0_RX_RS4XX_N	
Pin 3	UART0_TX_RS4XX_P	UART0 TX. For RS485 mode, connect to UART0 RX
Pin 4	UART0_TX_RS4XX_N	
Pin 5	GND	Ground
Pin 6	GND	
Pin 7	UART1_RX_RS4XX_P	UART1 RX. For RS485 mode, connect to UART1 TX
Pin 8	UART1_RX_RS4XX_N	
Pin 9	UART1_TX_RS4XX_P	UART1 TX. For RS485 mode, connect to UART1 RX
Pin 10	UART1_TX_RS4XX_N	
Pin 11	UART2_RX_RS4XX_P	UART2 RX. For RS485 mode, connect to UART2 TX
Pin 12	UART2_RX_RS4XX_N	
Pin 13	UART2_TX_RS4XX_P	UART2 TX. For RS485 mode, connect to UART2 RX
Pin 14	UART2_TX_RS4XX_N	
Pin 15	GND	Ground



NAME	DESCRIPTION	CONNECTOR PINS	DIFF. VOLTAGE		LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART0_RX_RS4XX_P	UART0 RX	1	0.2	12	-7	-	-	12	-60	+60
UART0_RX_RS4XX_N		2			-7	-	-	12	-60	+60
UART0_TX_RS4XX_P	UART0 TX	3	2.0	3.6	0	0.4	2.4	3.6	-20	+20
UART0_TX_RS4XX_N		4			0	0.4	2.4	3.6	-20	+20
UART1_RX_RS4XX_P	UART1 RX	7	0.2	12	-7	-	-	12	-60	+60
UART1_RX_RS4XX_N		8			-7	-	-	12	-60	+60
UART1_TX_RS4XX_P	UART1 TX	9	2.0	3.6	0	0.4	2.4	3.6	-20	+20
UART1_TX_RS4XX_N		10			0	0.4	2.4	3.6	-20	+20
UART2_RX_RS4XX_P	UART2 RX	11	0.2	12	-7	-	-	12	-60	+60
UART2_RX_RS4XX_N		12			-7	-	-	12	-60	+60
UART2_TX_RS4XX_P	UART2 TX	13	2.0	3.6	0	0.4	2.4	3.6	-20	+20
UART2_TX_RS4XX_N		14			0	0.4	2.4	3.6	-20	+20

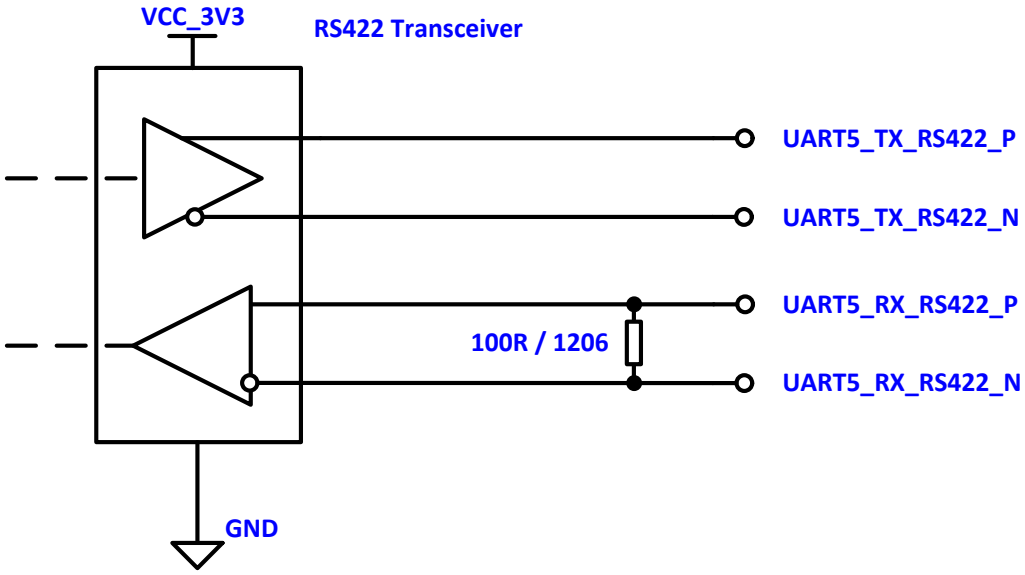
Note: This denotes the peak AC current into the AC termination. Steady state DC current is max. +/-125µA.

3.5 UART 3-5 connector

This connector provides two RS422 UART interfaces that can also be used in RS485 configuration through connecting input and output circuits to one signal pair. For a detailed interface specification of the UART3 and UART4 interfaces, please see the description in section 3.4, the interfaces are identical between the two connectors. UART5 is configured as a higher speed UART with higher drive capability and resistive input termination. Due to power dissipation limits, UART5 only supports 3.3 V levels and not full RS422 levels.

nanoD15 Socket Connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	UART3_RX_RS4XX_P	UART3 RX. For RS485 mode, connect to UART3 TX
Pin 2	UART3_RX_RS4XX_N	

Pin 3	UART3_TX_RS4XX_P	UART3 TX. For RS485 mode, connect to UART3 RX
Pin 4	UART3_TX_RS4XX_N	
Pin 5	GND	Ground
Pin 6	GND	
Pin 7	UART4_RX_RS4XX_P	UART4 RX. For RS485 mode, connect to UART4 TX
Pin 8	UART4_RX_RS4XX_N	
Pin 9	UART4_TX_RS4XX_P	UART4 TX. For RS485 mode, connect to UART4 RX
Pin 10	UART4_TX_RS4XX_N	
Pin 11	UART5_RX_RS4XX_P	UART5 RX. Higher speed UART, but limited to 3.3 V signaling levels
Pin 12	UART5_RX_RS4XX_N	
Pin 13	UART5_TX_RS4XX_P	UART5 TX. Higher speed UART, but limited to 3.3 V signaling levels
Pin 14	UART5_TX_RS4XX_N	
Pin 15	GND	Ground



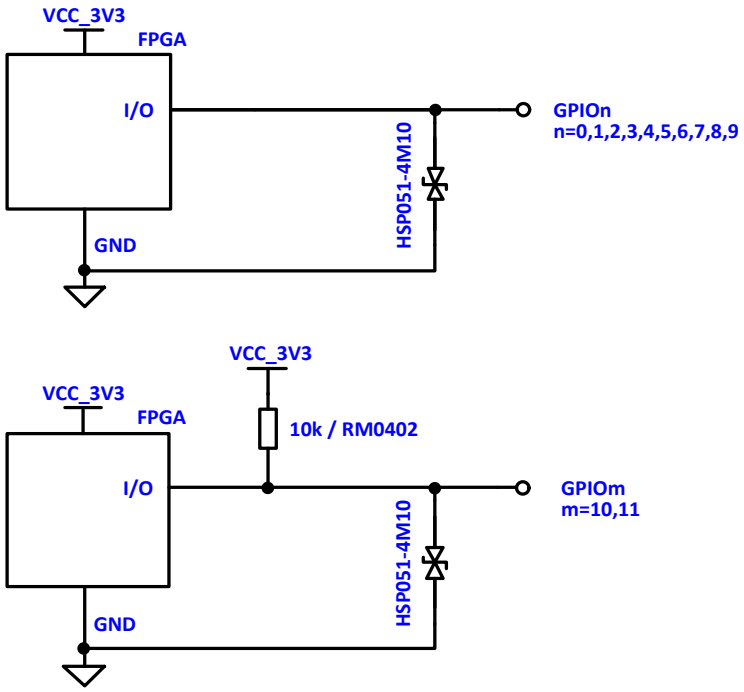
NAME	DESCRIPTION	CONNECTOR PINS	DIFF. VOLTAGE		LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
UART5_RX_RS422_P	UART5 RX	1	0.2	3.5	-7	-	-	12	-35	+35
UART5_RX_RS422_N		2			-7	-	-	12	-35	+35
UART5_TX_RS422_P	UART5 TX	3	2.0	3.6	0	0.4	2.4	3.6	-20	+20
UART5_TX_RS422_N		4			0	0.4	2.4	3.6	-20	+20

3.6 DIGITAL connector

This connector provides several digital I/O interfaces and an external interface for a PPS time synchronization signal.

nanoD25 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	GPIO0	LVTTL digital inputs/outputs
Pin 2	GPIO1	
Pin 3	GPIO2	
Pin 4	GPIO3	
Pin 5	GPIO4	
Pin 6	GPIO5	
Pin 7	GPIO6	
Pin 8	GPIO7	
Pin 9	GPIO8	
Pin 10	GPIO9	
Pin 11	GPIO10	LVTTL digital input/output with 10kΩ pull up resistor for open drain usage
Pin 12	GPIO11	LVTTL digital input/output with 10kΩ pull up resistor for open drain usage
Pin 13	GND	Ground
Pin 14	SPI_MISO	NOT USED
Pin 15	SPI_MOSI	
Pin 16	SPI_CLK	
Pin 17	I2C_SCL0	NOT USED
Pin 18	I2C_SDA0	
Pin 19	I2C_SCL1	
Pin 20	I2C_SDA1	NOT USED
Pin 21	I2C_SCL2	
Pin 22	I2C_SDA2	
Pin 23	PPS_INPUT_RS422_N	PPS input, differential RS422 signal for time synchronization
Pin 24	PPS_INPUT_RS422_P	
Pin 25	GND	Ground

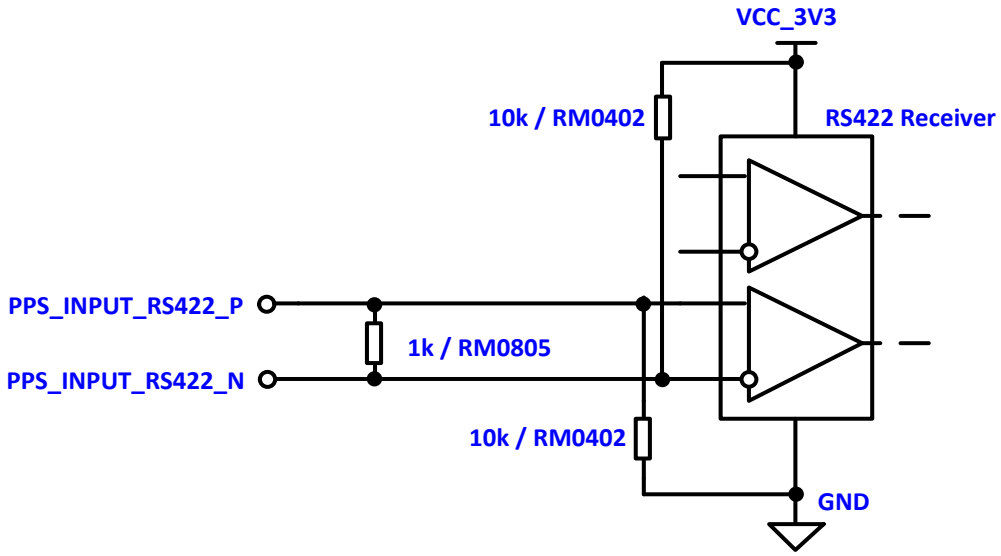
3.6.1 GPIO Interface



NAME	DESCRIPTION	CONNECTOR PINS	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
GPIOn out	GPIO configured as output	1,2,3,4,5,6,7, 8,9,10	0	0.4	2.4	3.45	-12	12
GPIOn in	GPIO configured as input	1,2,3,4,5,6,7, 8,9,10	-0.3	0.8	2.0	3.45	-0.01	0.01
GPIOn out	GPIO w/ pull-up configured as output	11,12	0	0.4	2.4	3.45	-12	12
GPIOn in	GPIO w/ pull-up configured as input	11,12	-0.3	0.8	2.0	3.45	-0.01	0.29

3.6.2 PPS Input Interface

The PPS pulse is required to be a positive pulse with 1 µs to 1 ms duration.



NAME	DESCRIPTION	CONNECTOR PINS	DIFF. VOLTAGE	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
PPS_INPUT_RS422_N	PPS INPUT	23	0.2	-7	-	-	7	-0.7	+1.2
PPS_INPUT_RS422_P		24		-7	-	-	7	-0.7	+1.2

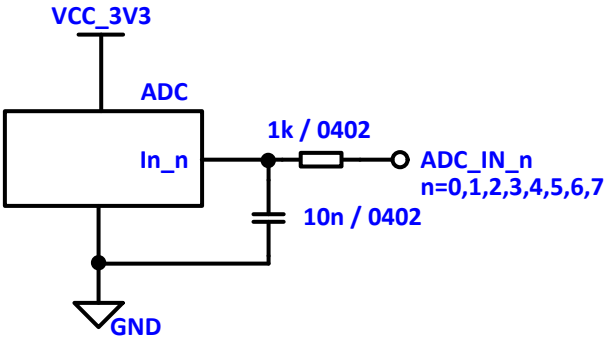
3.7 ANALOG connector

This connector provides 10 analog input channels as well as several digital IOs.

Note: The maximum input voltage on the analogue inputs for correct digitization is 2.05 V. The electrical absolute maximum rating is 3.4 V.

nanoD25 Socket		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	ADC_IN_0	Analog inputs to ADC with 2.5V reference and buffer
Pin 2	ADC_IN_1	
Pin 3	ADC_IN_2	
Pin 4	ADC_IN_3	
Pin 5	ADC_IN_4	
Pin 6	ADC_IN_5	
Pin 7	ADC_IN_6	
Pin 8	ADC_IN_7	
Pin 9	BIAS	2.5V analog reference voltage with buffer, output bias current used is max 5 mA, see section 3.7.3
Pin 10	BIAS	2.5V analog reference voltage with buffer, output bias current used is max 5 mA, see section 3.7.3
Pin 11	GPIO12	LVTTL digital inputs/outputs
Pin 12	GPIO13	
Pin 13	GPIO14	
Pin 14	GND	Ground
Pin 15	GND	
Pin 16	GND	
Pin 17	GND	
Pin 18	GND	
Pin 19	GND	
Pin 20	GND	
Pin 21	GND	
Pin 22	BIAS	2.5V analog reference voltage with buffer, output bias current used is max 5 mA, see section 3.7.3
Pin 23	BIAS	2.5V analog reference voltage with buffer, output bias current used is max 5 mA, see section 3.7.3
Pin 24	GPIO15	LVTTL digital input/output
Pin 25	GND	Ground

3.7.1 Analog Input Interface



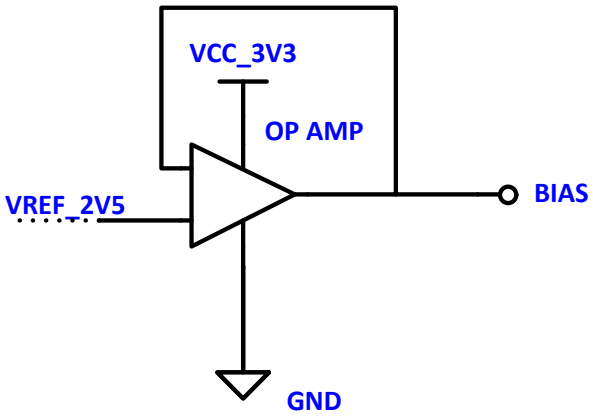
NAME	DESCRIPTION	CONNECTOR PINS	LOW VOLTAGE		HIGH VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [V]	MAX [V]	MIN [nA]	MAX [nA]
ADC_IN_n	Analog input channel	1, 2, 3, 4, 5, 6, 7, 8	0	-	-	3.4	-2	+2

Note: As described in section 3.7, the maximum resolvable input voltage is 2.05 V

3.7.2 GPIO Interface

For the GPIO Interface, please see the description in chapter 3.6 as the interfaces are identical to the interfaces without pull-up resistors.

3.7.3 Bias voltage 2.5V



NAME	DESCRIPTION	CONNECTOR PINS	VOLTAGE		CURRENT	
			MIN [V]	MAX [V]	MIN [mA]	MAX [mA]
BIAS	2.5V Bias Voltage	9, 10, 22, 23	2.48	2.52	-10	+10

Note: The output current capability is for all bias pins combined

3.8 JTAG-RTL connector

This connector provides an interface to program the FPGA during manufacturing.

ST60-10P connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	GND	Interface to Microsemi FlashPro programmer
Pin 2	RTL-JTAG-TDI	
Pin 3	RTL-JTAG-TRSTB	
Pin 4	VCC_3V3	
Pin 5	VCC_3V3	
Pin 6	RTL-JTAG-TMS	
Pin 7	Not connected	
Pin 8	RTL-JTAG-TDO	
Pin 9	GND	
Pin 10	RTL-JTAG-TCK	

3.9 DEBUG-SW connector

This connector provides the programming interface for the AAC debugger.

ST60-18P connector		
PIN #	**SIGNAL NAME**	**DESCRIPTION**
Pin 1	ETH-DEBUG-RESET	Interface to AAC debugger
Pin 2	ETH-DEBUG-DETECT	
Pin 3	ETH-DEBUG-SYNC	
Pin 4	ETH-DEBUG-TX	
Pin 5	ETH-DEBUG-RX	
Pin 6	ETH-DEBUG-MDC	
Pin 7	ETH-DEBUG-MDIO	
Pin 8	ETH-DEBUG-CLK	
Pin 9	GND	
Pin 10	DEBUG-JTAG-TDI	
Pin 11	DEBUG-JTAG-RX	
Pin 12	DEBUG-JTAG-TX	
Pin 13	VCC_3V3	
Pin 14	DEBUG-JTAG-TMS	
Pin 15	VCC_3V3	
Pin 16	DEBUG-JTAG-TDO	
Pin 17	GND	
Pin 18	DEBUG-JTAG-TCK	

3.10 Add-on connector

The Sirius OBC has a Hirose FX8C 60-pin board-to-board connector allowing add-on boards to be fitted to the unit. No signals are present on this connector by default, but ÅAC can upon request develop customer specific add-ons using this connector.

3.11 Power consumption

Nominally: < 1.5W

Maximum power consumption is dependent on the numbers of interfaces used and the connected equipment.

3.12 Protection

All inputs and outputs of the Sirius OBC have ESD protection. This makes the Sirius OBC robust against unintended damage to the unit through static discharge. Regardless, the units shall only be operated in an ESD safe area.

3.13 Grounding

All Sirius products are designed with separated power/signal ground and chassis ground, connected only capacitively and with a high impedance bleed resistor. When assembled in the spacecraft, the chassis ground shall be bonded to the structure using the grounding point on the case. The grounding point is an M3 threaded hole. If several Sirius units are assembled in a stack configuration, only one of the grounding points need to be used.

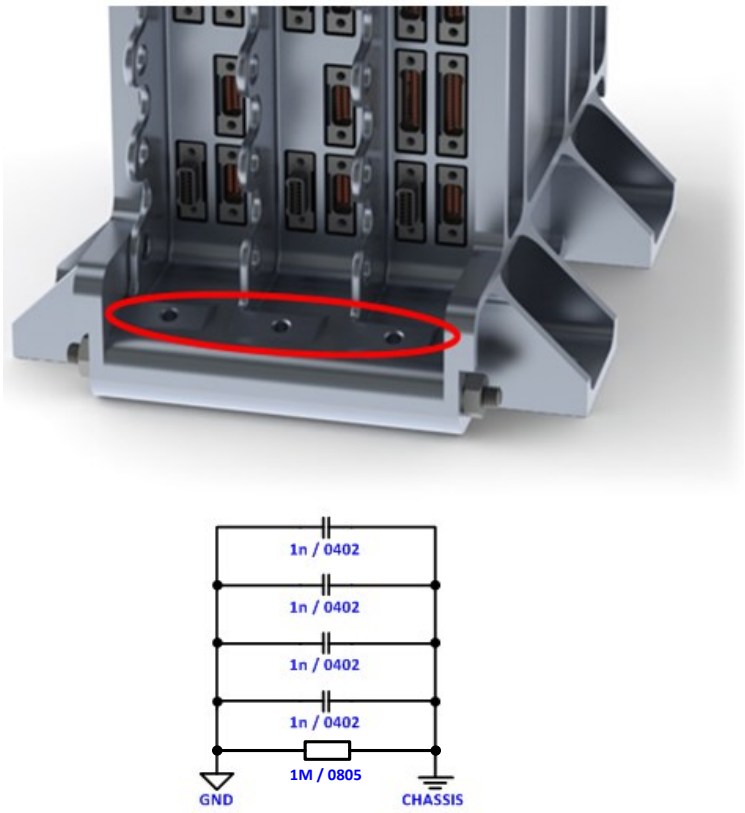


Figure 5 - The Sirius products ground and chassis concept

3.13.1 Protection of unused connectors

It is recommended to cover any connectors which are not used in flight. This can be done either through attaching small metal cover plates, or through filling the unused connector with epoxy. The recommended epoxy for this application is 3M Scotchweld 2216. When epoxyfilling the connectors, the Sirius product should be placed in such a way that the connector forms a bathtub, preventing the epoxy from pouring out of the connector during curing.